

LIMITATIONS OF A TRUE RANDOM NUMBER GENERATOR IN A FIELD PROGRAMMABLE GATE ARRAY

THESIS

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Abstract

Random number generators are used in many areas of engineering, computer science, most notably in simulations and cryptographic applications. There are true random number generators (TRNG) and pseudo random number generators (PRNG).

Only a true random number generator is secure because the output bits are non-repeating and non-reproducible. As society has become more dependent on electronic technology the need for true random number generators has increased due to processes that require encryption in everyday use. A fast true random number generator on a field programmable gate array presents digital designers with the ability to have the generator on chip. Since random bits do not have to be brought into the processes from an outside source, they cannot be compromised.

An oscillator sampling technique has proved to be an effective TRNG in a Xilinx FPGA. This research examines how the time of the differences in period of the two oscillators, the size of the jitter zone, and whether sampling on the rising and falling edge of the oscillator rather than just the rising edge affects the randomness of the TRNG.

The proportion of the size of the jitter zone compared to the period difference between the two oscillators limits the performance of this technique. As the jitter zone gets larger, the proportion of the jitter zone to the difference in periods of the oscillators must increase for the output to remain random. Increasing the output rate by sampling on the rising and falling edge instead of only the rising was not effective. The output was random for only a jitter zone of 24 ps with a period difference of 50 ps and 100 ps.

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I. Introduction

1.1 Background

Random numbers are used for many different applications varying from gaming to decision making, cryptography, simulations and sampling [Knu69]. Random number generators are found everywhere, from video games that children play, to computer simulations and encryption protocols. A football computer game may use a random number generator to decide whether the player on the video game will catch the ball or drop it. Random numbers are needed for encryption in online transactions and Internet security. A random number generator for encryption purposes needs to provide security and must not be repeatable, where as a random number generator for a video game does not have a need to be as strong as those used for encryption or national security. How random the output of a random number generator needs to be depends on the purpose for which it is used. What makes a good random number generator? True random numbers are a sequence of digits that cannot be predicted or reliably reproduced [Sch94]. A sequence of random numbers are numbers that are independent and contain properties of a particular distribution [Knu69]. A true random sequence of numbers cannot be compressed [Tho03]. Randomness is not something that can be manufactured. Different applications that have a need for randomness obtain their random numbers from many types of sources. Some sources produce true random numbers; other sources produce pseudo random numbers.

The need for random numbers or random outcomes has been around since the earliest recorded times in history. One method recorded for choosing random numbers in early history was by throwing and object in the air and observing on which side it lands. This method is often used today when rolling a die or tossing a coin. The coin toss is observed at the beginning of football games in deciding which team will perform the opening kick-off. Another method of random number generation, recorded and currently used in areas such as lotteries, selects an item out of a container or urn of well mixed or shaken items. Choosing an item out of an urn is the method of randomness treated, in many books on statistics and probability, as one of the simplest methods of randomness.

A true random number generator typically uses some sort of physical process as the source of randomness. A pseudo random number generator is often an algorithm and a seed value used to produce an output. A true random number generator uses more equipment and is more difficult to implement than a pseudo random number generator, therefore there are more PRNG's than TRNG's.

True random number generators are preferred for use in cryptographic applications. The need for encryption is greater today with the increased use of the Internet. Encryption is needed for checking email, managing bank accounts, purchasing items online, filling out job and college applications, filing tax returns, and sending digital photographs to family. TRNG's are desirable for the secure encryption they produce since the random numbers are not reproducible. If given a number or series of

numbers in a sequence output from a TRNG, the sequence cannot be used to predict future sequences that are produced by the same generator.

1.2 Goals of Research

One approach for producing cryptographically secure random numbers uses multiple oscillators and the random jitter of those oscillators' signals to produce true random numbers. A digital circuit in a field programmable gate array can be used to sample oscillator signals. This circuit is small enough to put on an FPGA along with an application in which the generator will be used. The limitations of the TRNG need to be considered and tested when using the TRNG on an FPGA to ensure the output remains random. The goal of this research is to determine the limits on the width of the jitter zone. There are many different types of FPGA's and different ranges of jitter on the signals produced between different chips and even on the same chip. Furthermore, the difference in periods between the two sampling oscillators is considered. Finally, a method of increasing the output of the generator is considered by sampling on both the rising and falling edge of the oscillator rather than just the rising edge.

1.3 Documentation overview

This document contains five chapters. This chapter gives a background of random numbers and the extensive use of random number generators. It also defines the purpose of the research to find jitter and frequency limitations on the oscillators used for the TRNG and to see if the generator speed can be increased by sampling on rising and falling edges of the signal. Chapter 2 is a literature review that discusses the background

of random numbers and the different types of random number generators. It also looks at the current research of random number generators in field programmable gate arrays.

Chapter 3 lays out the methodology for conducting the research for this thesis. Chapter 4 presents the results and analysis of the experiments performed. Chapter 5 contains the conclusions of the research and identifies future research areas.

II. Literature Review

2.1 Sources of Randomness

True sources of randomness come from unpredictable physical sources. There are physical sources that are very good at generating random sequences, but the sources are often very slow, or take an extensive amount of hardware to obtain the random sequence [ChJ99]. "Quantum Randomness is based on quantum events such as splitting atoms, deriving randomness through molecule movement, division of cells and such. This is expressed as the most random occurrences known to date, which means nobody has been able to discern any patterns so far." [Tho03] Other physical sources used for TRNGs are the time it takes for an atom to decay in radioactive material, thermal noise from a diode or precision resistor, background noise in a computer room, digital captures of the movement of the material in a lava lamp and signal jitter. It is important that the physical source of randomness be unpredictable and without bias. Humans actions may seem random at times but do not make a good source of randomness. Humans are actually very predictable and tend to have patterns of actions and therefore exhibit bias.

Randomness is often referred to as entropy. Entropy is a quantitative measure of the uncertainty of an outcome [Leo94]. A sequence with high entropy means it is more difficult to predict a number in the sequence from the preceding numbers than in a sequence with a low entropy number. A high entropy value does not necessarily guarantee that a sequence is random, however. A compressed image file has high entropy but there is a specific configuration to the data bits [Haa99].

Random number generators (RNG) use the physical sources of randomness to produce sequences of random numbers. RNGs generally fall into two categories: true random number generators (TRNG) and pseudo random number generators (PRNG). There is also a third category referred to as hybrid number generators.

2.2 True Random Numbers

Random numbers are said to be True Random Numbers if they are non-deterministic, unbiased, independent, uncompressible, and are able to pass a series of statistical tests [Tka02] some of which are described later. An unbiased sequence of random numbers is a sequence in which each possible number generated is equally probable to appear in the sequence. A bit generator can produce zeroes or ones.

Therefore, since there are only two possible outputs from the generator, an unbiased sequence of bits will have a probability of 0.5 of being a one and a probability of 0.5 of being a zero. Whether a random number generator is determined to be a "good" random number generator largely depends on the intended use of the random numbers [Hel98].

A "good" random number generator produces results that are acceptable in a variety of different applications [Hel98]. True random numbers have a variety of applications such as simulation and testing, statistical sampling, numerical analysis and cryptography [YSV04].

Random numbers are used in simulations and testing to indicate the occurrence of a natural event [Knu69]. Simulations using random numbers are used in many different fields such as operations research, physics, and engineering. Simulations in the operations research field requiring random numbers include queuing theory and process

modeling simulations. Random numbers used in queuing simulations can represent the variability seen in service times in a line at a bank or store, for example. Random numbers in process modeling simulations can, for instance, be used to model demand patterns in inventory process models. Examples of physics and engineering simulations include simulations of particle movement [Knu69], and random noise in communication transmissions.

Statistical sampling is used when it is unreasonable to observe all cases. A random sample is often used to determine the demographics of a particular area, when trying to determine a winner in an election before the votes are counted, or when trying to determine how fast a disease is spreading through the cells of a body. If the sample collected is not a truly random sample then the conclusions reached from analyzing the sample could be very different than the actual population.

A true random sequence of numbers is extremely important when creating a cryptographic key. The only unbreakable key is known as a one-time pad in cryptographic terminology and is used only once. Other keys that are not truly random can be deciphered and often result in a breach of security.

A true random number generator samples an entropy source to obtain random bits. Some of the hardware-based random number generators include observing the decay of atoms in radioactive material, thermal noise from a diode or precision resistor, atmospheric noise from a radio, background noise in a room, and frequency jitter in a free running oscillator [MOV97]. The particular time an atom in radioactive material decays is unknown and there is no pattern in the time between one atom and another decaying. Therefore, the time between atoms decaying is considered a good source of true

randomness [McG02] but can only produce bits at a rate of several hundred bits per second [FDS04]. Thermal noise from a precision resistor or diode is also fairly slow at random bit generation [ChJ99]. Thermal noise uses the voltage from noise compared to a reference voltage to produce random bits. If the noise voltage is higher a '1' is produced, a '0' if lower.

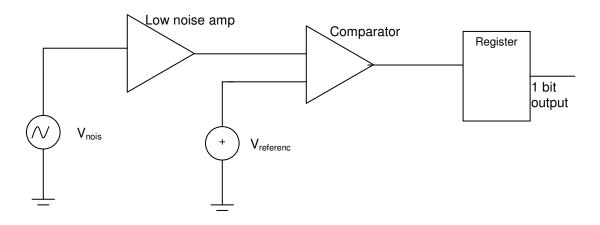


Figure 1. A One Bit True Random Generator [ChJ99]

Figure 1 is a true random bit generator based on the thermal noise of a precision resistor. The thermal noise true random bit generator uses hardware that preserves the thermal noise, amplifies it and guards it against any outside influences. The thermal noise (V_{noise}) is amplified and sent through a comparator where V_{reference} is the reference voltage. The output of the comparator is sampled and latched into a digital register. The output of the register is the random bit observed from the thermal noise random bit generator [ChJ99]. A generator such as Figure 1 should not be used as a source of randomness in high security applications such as cryptography since the random signal could be observed in the path from the analog components to the discrete component.

A signal from a free running oscillator has a particular frequency. Figure 2 shows a oscillator signal with an unknown area called a jitter zone. It is unknown whether the signal will be high or low in the jitter zone. The jitter zone provides a good source of randomness when the oscillator signal is sampled at a frequency close to the frequency of second sampling oscillator. Figure 2 shows the jitter zone only on the rising edge of each cycle. There is also a jitter zone on the falling edge of the each cycle.

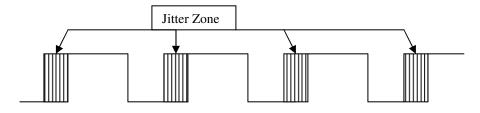


Figure 2. Frequency Jitter

A frequent problem in true random number generators is the sequence of numbers is often biased. In other words, the distribution of numbers is not uniform [Knu69] and therefore does not pass statistical tests for an unbiased source. Von Neumann created a simple unbiasing procedure for random binary bits. Bits are paired together; if the two bits are equal they are thrown out. If the first bit in the remaining pairs is a 1, then a 1 is used as the result while if the first bit of the pair is a 0, then a 0 is the result as seen in Figure 3 [Dav00]. The Exclusive OR (XOR) corrector is another unbiasing procedure. Each pair of bits is exclusive OR'ed together. If the bits are the same the output is a 0 and if the bits are different the output is a 1. The XOR Corrector, shown in Figure 3, produces half as many bits as the original random bit stream. The Von Neumann Corrector can result in as few as twenty-five percent of the original bit stream.

Recall that an unbiased random sequence cannot be compressed. Therefore, a compression procedure can also be used to unbias the bits of a random number generator.

A compression unbiasing procedure, however, also reduces the number of random bits. If the sequence of random bits is compressed to a great extent, the number of available bits can be significantly reduced.

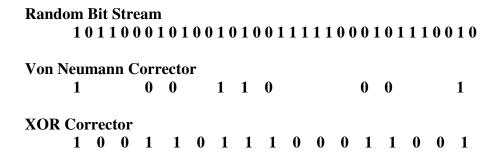


Figure 3. Von Neumann and Exclusive Or Corrector for Unbiasing Random Sequences.

2.3 Pseudo Random Numbers

A sequence of pseudo random numbers is a sequence of numbers that are produced deterministically [Knu69]. A pseudo random number generator may pass all the tests for creating a random sequence. However, since the sequence is produced deterministically, it will produce the same sequence if the generator is given the same initial seed [Koh04]. A good pseudo random number sequence appears to be random and cannot be distinguished from true random sequences statistically [SKP02]. Although the sequence may pass statistical tests for randomness it eventually repeats. Perhaps, it will not repeat for a long time but it will eventually repeat. The majority of random number generators used are pseudo random number generators which are simply deterministic mathematical algorithms [Knu69] usually implemented in software. However, the increase of transistors that can be placed on digital chips has made it possible to

implement many algorithms that form "good" pseudo number generators in hardware. A true random sequence of numbers could not be generated on a deterministic computer, because it needs to sample a high entropy physical source to obtain truly random numbers. Furthermore, a pseudo random number generator should not be used for encryption purposes unless it is considered a cryptographically secure pseudo random number generator (CSPRNG). If the mathematical algorithm and the seed for the pseudo random number generator is known the outcome can be predicted. An output is more difficult to predict if the seed is large and is generated from an entropy source that makes it difficult to predict. A random number generator is considered cyptographically secure if the generator is "computationally infeasible to predict the next output" [Koh03].

Many pseudo random number generators that have been tested are determined to be "good" generators. A few of the commonly used pseudo random number generators include the Linear Congruential Generator [Knu69], Linear Feedback Shift Register [TLL03], Lagged Fibonacci Generator [Cod96], and the Cellular Automata RNG (a hardware-based generator).

The Linear Congruential Generator (LCG) is a commonly used pseudo random number generators [Knu69]. The LCG equation is

$$X_{n+1} = (a X_n + b) \bmod m \tag{1}$$

where m is the modulus, a is the multiplier, b is the increment and X_n is the starting value or seed value. The modulus operator, written mod m in the equation, takes the value preceding the operator and divides it by the modulus m and returns the remainder. The modulus should be greater than X_n , a, and b, [Knu69]. The modulus should be a large, prime number since the period of the sequence is always less than or equal to the

modulus [Knu69]. The LCG is considered a "good" pseudo random number generator if the number of bits used and the constants are chosen such that the output of the LCG has a long period.

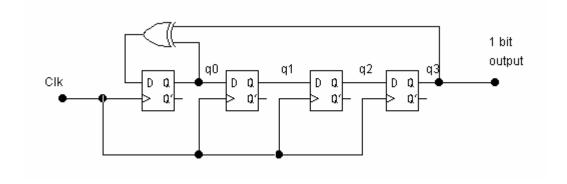


Figure 4. Four Bit Linear Feedback Shift Register

Figure 4 is a four bit linear feedback shift register (LFSR) pseudo random number generator. A LFSR generator, with N bits has a maximum repeat length of 2^N -1 cycles [ChJ99]. Therefore, the four bit generator in Figure 4 has a maximum repeat length of fifteen. The LFSR is initialized with any four bit sequence except all zeroes. If the registers are initialized with zeroes the output will always be zero. If the registers are initialized with 1010 for reg0, reg1, reg2, reg3, the output sequence, first to last bit out, is 0101100100011110 at which point the sequence will repeat. If 64 registers are used, and the registers are clocked at 1 gigahertz then it would take more than 500 years before the cycle of output numbers would repeat [ChJ99]. The input to the first register in Figure 4 is the output of an XOR gate whose inputs (or taps) are q0 and q3. The tap choice is important to obtain the maximum cycle length. The taps are determined by a recurrence equation $X_n = a_1(X_{n-1}) \oplus a_2(X_{n-2}) \oplus \dots \oplus a_m(X_{n-m})$ where \oplus is the exclusive OR operator. The constants a_i are a predetermined value of zero or one [ChJ99]. Many papers, textbooks and application notes contain tables listing taps that produce the

maximum cycle length and prevent the LFSR from entering a state with the registers all containing zeros. A LFSR can easily be implemented in digital hardware using registers and an exclusive or gate. It is best to seed the LFSR with an initial value that comes from a physical or secret entropy source depending on the use for the generator. The LFSR is not recommended as a PRNG in software because it has poor random qualities compared to the LCG and the lagged Fibonacci generator [Cod96] but it much easier to implement in hardware than most of the software generators. The LFSR is basically the Fibonacci generator using the exclusive OR operation. It give worse statistical properties than the additive or multiplicative LFG because the exlusive OR is a simple operation.

A lagged Fibonacci pseudo random number generator equation is

$$X_n = (X_{n-r} \oplus X_{n-s}) \bmod m \tag{2}$$

where Θ can be addition, subtraction, multiplication, or a bitwise exclusive OR and r, s, m are constants. The constants r and s provide the lag in the sequence. The generator is a multiple bit generator unlike the LFSR that generates one random bit at a time. An additive lagged Fibonacci generator requires a large lag to achieve randomness that passes the statistical tests, which in turn, requires more memory if implemented in software or more circuitry if implemented in hardware. A multiplicative lagged Fibonacci generator can have a significantly smaller lag to produce random numbers but in hardware it still requires memory to hold the numbers. Multiplication requires more hardware than addition. The first two numbers for a sequence from a Fibonacci generator must be supplied and generally m is usually chosen as a power of two. Multiplication is the best operator for randomness in the lagged Fibonacci generator but if speed is a concern addition or subtraction is used [Cod96].

The cellular automata random number generator is non-software based generator which consists of an array of cells. Each cell has a particular state. The number of possible states for a single cell to have is k. If binary digits are used then k=2, each cell will either be a one or a zero. The state of a cell is a function of the state of N neighboring cells [STC02]. A predetermined set of rules specifies how the N neighbors are chosen.

0	1	2	3
1	0	1	1
4	5	6	7
0	0	0	1
8	9	10	11
1	1	0	0
12	13	14	15
0	1	0	1

Figure 5. A four by four array of cells

Figure 5 is a four by four array of numbered cells. Each cell holds a single binary digit (the cells could also hold a variety of colors). An individual cell uses its N neighbors to determine what value it will hold at the next time increment. For N=2, each cell uses two of its neighbors and a given rule to determine the cells contents during the next time interval. The edges of the neighborhood "wrap" when looking at neighbors [STC02]. For example, in Figure 5 neighbors for cell 1 could be cell 2 and cell 13. The number of possible implementation for a two state cellular automata is $2^{2^{n}N}$. Since N=2, there are 16 possible implementations.

2.4 Hybrid Random Numbers

Another type of random number generator is the Hybrid Random Number Generator or the combined generators. There are two basic types of hybrid generators. One uses a true random number generator to seed a pseudo random number generator, and the other combines two or more pseudo random number generators to produce a sequence better at passing the statistical tests. A hybrid generator might consist of two linear congruential generators, or a linear congruential generator with a lagged Fibonacci generator. The two generators should produce a good random sequence and tested to make sure the resulting sequence is indeed random. If two of the same types of pseudo random number generators are used, each generator must be initialized with a different seed value to avoid correlation.

The RAND function in Matlab 5 by Mathworks is a hybrid number generator. It uses a Fibonacci random number generator to generate a 32 bit floating point number combined with a shift register generator that generates integer values [Mat07].

Motorola has a hybrid generator that uses a 43 bit linear feedback shift register and a 37 bit cellular automata shift register (CASR). Each generator uses a different oscillator and 32 of the output bits are selected and xor'ed together to produce the resulting random output sequence. The 43 bit LFSR alone has a maximum cycle length of 2^{43} -1 and a bias of approximately 2^{-43} . A random sequence should be unbiased. An unbiased sequence of random numbers is a sequence in which each possible number generated is equally probable to appear in the sequence. The 37 bit cellular automata shift register used alone has a maximum cycle length of 2^{37} -1 and a bias of 2^{-37} . When 32 bits of LFSR are XORed together with 32 bits of the CASR a maximum cycle length of 2^{80} - 2^{43} - 2^{-37} +1 is obtained with a bias of 2^{-80} [Tka02].

2.5 Testing for Randomness

A sequence is determined to be sufficiently random if it passes a series of quantitative tests [Knu69]. Two statistical tests used to determine the quality of random numbers include the Chi-square tests and the Kolmogorov-Smirnov test. The Chi-square test requires a large number of independent observations (Y_s) be made. The test statistic V is where n is the number of observed outcomes, k is the number of possible outcomes, k is the number of actual different outcomes, k is the expected probability of a particular outcome.

$$V = \frac{1}{n} \sum_{1 \le s \le k} \left(\frac{Ys}{ps} \right) - n \tag{3}$$

The value of V is compared with a Chi-square distribution table. V must be greater than or equal to the 99 percent entry or less than or equal to the 1 percent entry for the outcome to be considered random. A number of empirical tests can also be performed on sequences. Some common empirical tests are the Equidistribution test (the numbers of the sequence should be uniformly distributed), Serial test (pairs of successive numbers should be independent), gap test (a test to determine the length of gaps between numbers of a particular interval) [Knu69].

Although no series of tests can actually determine if a sequence is truly random, an analysis of the generator that produces the sequence must also be performed because it is possible for a pseudo random number sequence to pass all the statistical tests, but not be truly random [RSN01].

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The Diehard test is a series of rigorous statistical tests to determine randomness in pseudo random number generators [TLL03]. The Diehard is not well suited for measuring true random number generators. True random number generators typically produce random bits one at a time and the diehard tests are designed for generators that produce sequences that are 32 bits long [Dav00].

The National Institute of Standards and Technology (NIST) has assembled a statistical test suite for true random and pseudo random number generators intended for cryptographic applications. The NIST test suite has 15 statistical tests to test a binary sequence of arbitrary length. Each of the 15 tests produces a statistical value that is used to calculate a p-value. The p-value is a quantitative value that compares a perfectly random sequence with the sequence being tested. A p-value equal to one means that the sequence produced by a generator has complete randomness and a sequence having a pvalue of zero is entirely non-random. The NIST test suite consists of the following 15 tests: Frequency test; which tests the uniformity of the bits produced; a test for frequency of bits within an M size block; a Runs test to determine whether the transition between ones and zeros is too fast or too slow; a test for the longest run of ones in a particular size block is the expected length; a random binary matrix test which tests subsets of the sequence for linear independence from other subsets of the sequence; a spectral test to test for periodicity of the sequence; a non-overlapping template matching test; an overlapping template matching test; Maurer's Universal Statistical test which tests the sequence for compression without loss of information; the linear complexity test; the serial test; the approximate entropy test; the cumulative sums test; the random excursions

test; and the random excursions variant test [Bar00]. The effectiveness of the NIST test suite was determined using generators that were known to be "good" and "bad" [Bar00].

2.6 Current Research

Research in the area of random number generators is extensive because of their use and importance in many areas. There is an increased interest in implementing both pseudo random and true random number generators in Field Programmable Gate Arrays (FPGAs). FPGAs incorporate aspects of both Application Specific Integrated Circuits (ASIC) and processors. ASICs are high speed circuits but are relatively expensive to produce. They can only be used for one application and have a long production cycle. Processors, on the other hand, are very flexible since they can be programmed but are not designed for a specific application. They operate on a fixed data size and perform calculations sequentially. An FPGA, however, can be programmed to perform operations for a specific application in hardware but since they are programmable the design can be changed, multiple times, if necessary. They generally do not run as fast as an ASIC circuit but cost less and are suitable for prototyping [Wol04].

Many FPGA implementations of pseudo random number generators have been proposed. A single bit LFSR can be effectively implemented in a FPGA with little hardware using the FPGAs built-in look up tables (LUTs). The period of the generator grows exponentially with the addition of registers in the generator. A generator with a 32 bit LFSR repeats every 2³² bits or once every 4.2 billion bits [ChJ99]. Since an initial seed is needed for a LFSR, it is not acceptable for applications needing high security.

A parallel LFSR can serve as a multiple bit producing generator by using multiple copies of a single bit LFSR each with a different seed [ChJ99]. Another version of the LFSR is the multiple bit leap forward LFSR. It produces a multiple bit output from a single LFSR. The input to each of the registers is a combination of two or more registers outputs which require additional combinational logic gates for the generator circuit. The hardware for the lagged Fibonacci generator is similar to that of a LFSR, with two taps off the LFSR feeding back into hardware that performs multiplication, addition or subtraction on the two bits which are then fed back into the first register [ChJ99].

Sometimes a true random number generator seeds a pseudo random number generator on an FPGA. The true random number generator is implemented off chip and the generated random bits are used as a seed for an FPGA based pseudo random number generator. Physical sources such as physical noise are not available on a FPGA chip. If a physical noise random number generator is needed, the generator is constructed using analog components off chip (cf., Figure 1). However, a random number from an off-chip generator provides no security for applications such as cryptology or other secure applications as the signal can easily be intercepted as it is brought onto the chip.

True random number generator research using FPGAs has not been as extensive as that for pseudo random number generators. The need for true random number generators on FPGAs has become quite pronounced as security and cryptology are being implemented in FPGAs and random numbers for these applications must be unpredictable. The need for complete randomness and the security of the randomness has pushed research to embedded random number generators for FPGAs. However, digital circuits such as FPGAs lack the analog circuitry used in many true random number

generators leaving only clock jitter, free running oscillators and metastability as entropy sources [FDS04a].

Altera Stratix FPGAs have an analog Phase Lock Loop (PLL) that can be used as the physical source of randomness [FDS04a]. The PLL provides random fluctuations (or jitter) from the synthesized clock signal due to frequency changes caused by noise in the environment of the chip and variation in the supply voltage. The chip has an internal control to adjust the fluctuation in frequency but there remains a small fluctuation even after applying the controls. Jitter was measured up to 50 ps in the Altera Stratix device The jitter measured on an Application Specific Integrated Circuit (ASIC) board ranged from 3.5 ps to 10 ps and up to 140 ps on an APEX Field Programmable Logic Device (FPLD) [FDS04b]. The random bits are extracted from the jitter by feeding the original clock signal into two different PLLs. The synthesized clock signal from one of the PLLs samples the other synthesized signal. The output of the sampler is a string of consecutive zeros followed by a string of consecutive ones. The length of consecutive zeros or ones is different depending on the value of the PLL signal in the jitter zone. The sampled signal is put through a predetermined decimator based on the frequency of the PLL.

The Stratix FPLD family has up to eight Fast PLLs (FPLL) and Enhanced PLLs (EPLL). Four different configurations have been tested. The first used two FPLLs. The second configuration uses one FPLL and one EPLL. The third configuration uses just one EPLL, and the final test configuration uses two EPLLs. The fastest output bit rate and quality is produced when using two EPLLs. The random output passes the NIST tests at a speed of more than 1 M bits per second [FDS04a].

True random number generators have also been implemented in Xilinx FPGAs which do not have phase lock loops. The physical source of randomness is two ring oscillators. The idea is similar to the two synthesized signals used in the Altera PLL although Xilinx's FPGAs have delay lock loops (DLLs) instead of PLLs. DLLs reduce the clock skew but are not able to provide the quality frequency synthesis PLLs provide. Each ring oscillators consists of two transparent latches, an inverter and a buffer. The Xilinx FPGAs were tested at a frequency of 150 MHz. One oscillator samples the other oscillator, and it is important that the two oscillators be very close in frequency [Koh04]. The sampled output is either a one or a zero depending on what part of the cycle the signal is in when it gets sampled. A sample taken in the jitter zone (cf., Figure 2) can produce an output that is a one or a zero. It is unknown whether a sample taken in the jitter zone will be a one or a zero. The number of consecutive ones or zeros is counted, and the sample from the jitter zone is latched into a register. The counter is then reset. The random bits produced using the oscillators do not show any correlation to the other numbers in the sequence so an exclusive OR function is used to reduce any bias in the bits. The placement of the ring oscillators on the FPGA chip affects the speed of the oscillators due to temperature and delay in wires [Koh04]. Placement of the design on the FPGA board is important as speed is a concern.

2.7 Summary

Random number generators come in many different forms. There are True Random Number Generators, Pseudo Random Number Generators, and hybrids of the true and pseudo generators. The best generator depends on the intended application of

the random numbers. A true random number generator is used for high security applications and must produce numbers from a non-deterministic source. Sometimes a hybrid generator is sufficient for moderate security and can provide more generated random bits per second than a true random number generator. A hybrid generator must be thoroughly tested to make sure that the output produced is not less random than the individual generators used in the hybrid. A hybrid generator is used in many computer applications. Pseudo random generators produce sequences that appear truly random when a long period is constructed. Pseudo random generators are especially good for simulations, where security is not a concern.

III. Methodology

3.1 Problem Definition

True Random Number Generators (TRNG) are used in many applications. Many of the advances in current technology, such as the high speed internet and cellular communication, have produced a need for fast TRNGs that can be used for applications needing encryption.

3.1.1 Goals

The primary goal of this research is to develop a true random number generator (TRNG) for an FPGA and simulate it using Active HDL by Aldec. The TRNG is evaluated on the efficiency of producing a random bit stream and the quality of the randomness in that stream.

3.1.2 Approach and Hypothesis

A TRNG is simulated in Aldec's Active-HDL simulator and is implemented by sampling one simulated oscillator with a second simulated oscillator of an almost identical frequency. The sampling circuit captures a random bit when a clock oscillator samples a second clock oscillator in the jitter zone on the rising edge of the signal. A number of factors are varied and analyzed to determine the quality of a TRNG for a particular experimental configuration. The rate random bits are produced should increase by sampling the jitter zone on both the rising and falling edge of the oscillator rather than

on just the rising edge. The quality and speed at which the random bits are produced will likely be affected by a change in the difference in period of the two oscillators. The simulation produces jitter on the oscillators using the rng_lib.vhd file from opencores.org [Gei04]. A Gaussian distributed pseudo random number between 0-1 is produced by seeding the generator with three different ten digit values for each oscillator. Jitter on the oscillator signal has a Gaussian distribution. The value produced by the generator is used to determine the timing of the next edge of the clock signal. Different seed numbers are used for each of the six runs of each factor and for each of the two repetitions of the simulation.

3.2 System Boundaries

The System Under Test (SUT) in this research is the TRNG. Figure 6 shows the main parts of the TRNG. The TRNG is comprised of two ring oscillators, a sampling circuit, a control circuit and the system clock.

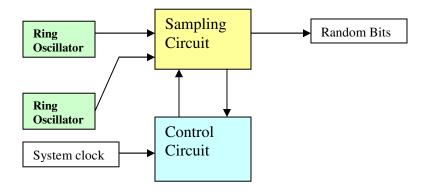


Figure 6. True Random Number Generator (System Under Test)

Each ring oscillator is constructed using a process in VHDL with the pseudo random number generator program rng_lib.vhd provided by opencores.org. The random number generator uses a combination of Tausworthe generators to determine the rising and falling of the oscillators edges for each particular jitter zone on an oscillator base frequency of 135 MHz. Three Tausworthe generators are used producing a pseudo random output with good statistical properties [TeL91]. The sampling circuit uses data flip flops (DFFs) and an inverter to sample the oscillators.

3.3 System Services

The system provides a single service of generating random bits. There are three possible outcomes of this service. The first possible outcome is no bits are produced from the system. Second, the system may produce bits, but the bits are not random. Third, bits are produced and they are random. The scope of this research is limited to the cases where bits are produced.

3.4 Workload

The workload for this system is straightforward. The system has three inputs.

The first input is the 50 MHz system clock signal which simulates the system clock on a Xilinx Spartan3 FPGA board. The second and third inputs are the two clock oscillators. The two oscillators are run at a base frequency of 135 MHz which is similar to that using hardware such as latches and inverters. The system produces one output: random bits.

3.5 Performance Metrics

One metric is used to evaluate the system: the quality of the bits produced by the system. The quality of the output bits is determined by testing the TRNG output using eight randomness tests from the National Institute of Standards and Technology (NIST) Statistical Test Suite for Random Number Generators [RSN01]. For this research a generator that produces a sequence of binary bits that pass six or fewer of the tests is considered non-random. If seven or eight tests are passed the generator is considered a possible true random generator and should undergo additional testing with a larger sample size to verify the initial results. A good random number generator will not pass all statistical tests all the time, some failures are expected [RSN01].

3.6 Parameters

3.6.1 System Parameters

The system parameters that may affect the performance of the system are:

- i) Frequency of the oscillators The base frequency of the oscillators will affect the output rate of random bits. If the frequency of the oscillators is increased the output rate will increase and if the frequency is decreased the output will decrease. The quality of the output may be affected by the ratio of the oscillator frequency to the width of the jitter zone.
- ii) The speed of the system clock The system clock controls the speed at which the data bits can be stored. If the oscillators are producing random bits at a faster rate than the bits can be written,

some of the bits will be dropped and may compromise the quality of the randomness. Increasing the speed of the system clock will allow all output bits to be collected.

iii) Sampling circuit implementation- This TRNG is for implementation on an FPGA board. If implemented on an ASIC (Application Specific Integrated Circuit) board it may have a slightly faster output. It would output bits at a slower rate if the user implemented it using discrete components.

3.6.2 Workload parameters

The workload parameters are:

- i) Width of the Jitter Zone The smaller the width of the jitter zone the more difficult it will be to capture a sample in the jitter zone area to produce a random bit.
- ii) Sampling trigger Sampling on the rising and falling edge of the signal versus just sampling on the rising edge. Sampling on both the rising and falling edge of the signal will produce a faster bit output rate but may affect the quality of the randomness of the bits.
- of the oscillators are the more often the sample will be taken in the jitter zone (i.e., the random bit) of the second oscillator. As the difference in period of the two oscillators increases, the time

- between random bit samples increases and if the difference becomes too large random bits may not be produced at all.
- iv) Increasing the number of ring oscillators Increasing the number of oscillators increases the speed of output bits. A greater number of output bits are produced by running multiple ring oscillator/sampling circuits in parallel.

3.7 Factors

Three factors are chosen for this experimental research. These factors and their levels are:

- 3.7.1 Width of the Jitter Zone (24 ps, 70 ps, 140 ps, 200 ps) A large jitter width of 200 ps is chosen based on Xilinx TechXclusives [Xil07] technical application note on jitter variation for the clock and data signal and Xilinx data sheets for the Spartan3 and Fischer's research and measurements of jitter [FDS04b].
- 3.7.2 Sampling Trigger (rising edge, rising and falling edge) The sampling trigger has two levels. The first level uses the rising edge of the first oscillator signal to sample the second oscillator. The second level uses the rising and falling edges of the first oscillator as a trigger to sample the second oscillator. A simplified version of a sampling technique that samples on the rising and falling edge of the sampling oscillator is seen in Figure 7. The random output rate should be twice the rate of sampling on only the rising edge.

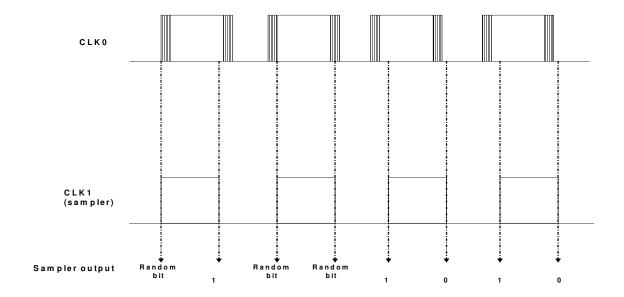


Figure 7. Rising a Falling Edge Triggered Sampling

3.7.3 Difference of periods of the oscillators – (24 ps jitter: 50 ps, 100 ps, 120 ps, 140 ps, 160 ps; 70 ps jitter: 250 ps, 300 ps, 320 ps, 350 ps, 436 ps; 140 ps jitter: 350 ps, 400 ps, 436 ps, 486 ps, 536 ps; 200 ps jitter: 436 ps, 486 ps, 536 ps, 586 ps, 630 ps) – A small difference in periods compared to the width of the jitter zone is the starting point for jitter zone width. The difference in the periods is increased until the output bits produced are no longer random. The output bits should no longer be random once the difference in periods is greater than twice the width of the jitter zone.

3.8 Evaluation Techniques

The evaluation technique is a simulation of bits produced by the random number generator and a statistical measurement of the quality of the randomness of the output

bits. The system is implemented using Aldec Active-HDL 6.3 software. The output bits written to an output text file.

3.9 Experimental Design

The design for this experiment is full factorial with two replications. Three factors are varied. The width of the jitter zone has four levels. The sampling trigger has two levels, and the difference in periods has five levels and two replications of each experiment are performed. Forty experiments are conducted (4 X 2 X 5 = 40), as seen in Table 1. Two replications yields eighty experiments. Each experiment collects six sets of data between 180 KB and 189 KB in size. The size of the data sets is limited to 189 KB for importing into Excel to exclusive OR consecutive bits removing any bias present. The size of the data file is also limited by search and replace program in Microsoft Word which is used to remove line returns between bits. The six data sets are combined to create one larger data set in the format needed for the NIST program. The NIST test suite returns a p-value and a proportion of the sequences that passed the statistical test. The p-value represents the probability that a sequence less random than the tested sequence was produced by an ideal RNG. Therefore, a high p-value indicates a "good" random sequence.

Table 1. Experiments Performed on TRNG

Experiment	Jitter Width	Sampling Trigger	Period Difference
1	24 ps	Rising edge	50 ps
2	24 ps	Rising edge	100 ps
3	24 ps	Rising edge	120 ps
4	24 ps	Rising edge	140 ps
5	24 ps	Rising edge	160 ps
6	24 ps	Rising and falling edge	50 ps
7	24 ps	Rising and falling edge	100 ps
8	24 ps	Rising and falling edge	120 ps
9	24 ps	Rising and falling edge	140 ps
10	24 ps	Rising and falling edge	160 ps
11	70 ps	Rising edge	250 ps
12	70 ps	Rising edge	300 ps
13	70 ps	Rising edge	320 ps
14	70 ps	Rising edge	350 ps
15	70 ps	Rising edge	436 ps
16	70 ps	Rising and falling edge	250 ps
17	70 ps	Rising and falling edge	300 ps
18	70 ps	Rising and falling edge	320 ps
19	70 ps	Rising and falling edge	350 ps
20	70 ps	Rising and falling edge	436 ps
21	140 ps	Rising edge	350 ps
22	140 ps	Rising edge	400 ps
23	140 ps	Rising edge	436 ps
24	140 ps	Rising edge	486 ps
25	140 ps	Rising edge	536 ps
26	140 ps	Rising and falling edge	350 ps
27	140 ps	Rising and falling edge	400 ps
28	140 ps	Rising and falling edge	436 ps
29	140 ps	Rising and falling edge	486 ps
30	140 ps	Rising and falling edge	536 ps
31	200 ps	Rising edge	436 ps
32	200 ps	Rising edge	486 ps
33	200 ps	Rising edge	536 ps
34	200 ps	Rising edge	586 ps
35	200 ps	Rising edge	630 ps
36	200 ps	Rising and falling edge	436 ps
37	200 ps	Rising and falling edge	486 ps
38	200 ps	Rising and falling edge	536 ps
39	200 ps	Rising and falling edge	586 ps
40	200 ps	Rising and falling edge	630 ps

3.10 Summary

The quality of randomness and speed of a true random number generator system are determined using the NIST Statistical Test Suite for Random Number Generators software. The TRNG is composed of two ring oscillators, a sampling circuit, and a control circuit and outputs a series of bits. The system's only service is to output random bits. There are three possible outcomes to the system: 1) no output bits, 2) outputs bits that are not random, 3) output bits that are random. Performance metrics are listed and three factors are chosen for this experiment. The factors are width of jitter zone, sampling trigger, and difference in period of the oscillators. A full factorial experiment design is used.

IV. Analysis and Results

4.1 Overview

The results and limitations of a simulation of a true random number generator in an FPGA using an oscillator sampling technique are presented in this chapter. Three factors of a random number generator were varied to determine the limitations of producing random numbers including the amount of jitter in the oscillators, the difference in period between the two oscillators, and whether the random bit is captured on the rising edge of the sampling oscillator or the rising and falling edge.

The simulation was run using Active-HDL 6.3 software by Aldec. The random numbers generated were output to a text file in ACSII. The random bits were analyzed using the National Institute of Standards and Technology (NIST) battery of tests to determine whether the sequences of binary bits were random. Enough data was collected to run eight of the fifteen NIST statistical tests for two sets of data. The NIST tests performed on the data were block frequency, non-overlapping templates, serial, approximate entropy, frequency, spectral DFT, runs and cumulative sums.

4.2 Interpretation of NIST results

The NIST test suite summarizes all tests run in a table in the *finalAnalysisReport* file which is in the algorithm testing folder in the NIST program. Table 2 is the output produced by one of the sets of data from the random number generator.

Table 2. NIST Results

NIST results for data set with rising edge sampling, 24 ps jitter zone and oscillators with a 140 ps difference in period. (Only five of the 148 output results for the nonperiodic-templates are shown. Full results available in Appendix A)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.1000 *	frequency
4	2	2	1	0	0	0	1	0	0	0.066882	0.9000 *	block-frequency
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.1000 *	cumulative-sums
9	1	0	0	0	0	0	0	0	0	0.000000	* 0.1000 *	cumulative-sums
5	0	1	0	0	2	0	2	0	0	0.004301	0.5000 *	runs
0	0	2	1	2	0	1	3	1	0	0.350485	1.0000	fft
3	3	0	1	0	0	1	1	0	1	0.213309	0.8000 *	nonperiodic-templates
3	0	1	1	0	0	2	1	1	1	0.534146	0.9000 *	nonperiodic-templates
3	2	0	0	1	0	1	2	1	0	0.350485	1.0000	nonperiodic-templates
0	1	0	1	1	1	1	3	2	0	0.534146	1.0000	nonperiodic-templates
0	1	2	1	0	2	0	1	1	2	0.739918	1.0000	nonperiodic-templates
5	1	1	1	0	1	0	0	1	0	0.017912	0.9000 *	apen
3	2	1	2	0	0	1	0	0	1	0.350485	1.0000	serial
1	2	1	0	1	1	0	2	1	1	0.911413	1.0000	serial

The NIST test suite produces a p-value for each of the tests run on the samples. A sample size of 10 was used for the data collected in this research. This p-value is not to be confused with the p-value in Table 2. "The p-value is the smallest level of significance that would lead to rejection of the null hypothesis H_0 with the given data [MoR99]." The null hypothesis for the NIST tests is the data collected is random. The NIST p-value is the probability a "perfect" RNG would have produced a sequence less random than the given sequence [RSN01] and can range from 0-1. These p-values are separated into ten distinct bins labeled C1-C10 (Table 2). The data being tested is divided into ten bit streams based on user input. The ten bit streams each result in a p-value and the number of p-values in each bin, recorded. A uniform distribution of p-values is desired for a random sequence. Column 11, in Table 2 is another p-value, from the chi-square test of the uniformity of the distribution of the individual p-values into the

bins. The individual p-values are not presented in the *finalAnalysisReport* table but are recorded in the individual result files for each test run in the NIST test suite. Column 12 is the proportion of the sequences that passed the statistical test (i.e., had a p-value greater than or equal to 0.01). A proportion of 0.895607 is the minimum pass rate for a sample size of 10 as defined by the NIST suite. The last column, in Table 2, is the test performed for that row of data.

The NIST tests suite uses 0.01 or greater as an acceptable p-value or significance level as do cryptographic applications [RSN01]. A significance level of 0.01 means that for one hundred binary sequences tested for the null hypothesis, one of the sequences is anticipated to be rejected as non-random [RSN01]. It is possible that the random number generator may appear random for a particular set of factor levels when it may not be. The test results give an idea of whether there are general conclusions that can be made about the random number generator due to the change in factors or if further data should be collected to obtain more precise conclusions. For the purpose of this research, a data set will be declared non-random when three or more of the eight NIST tests performed have a proportion level less than 0.895607.

4.3 Rising Edge Sampling

One oscillator signal was sampled on the rising edge of a second oscillator with a close, but slightly different period. Figure 8 shows the setup of the rising edge sampling circuit as used by Kohlbrenner [KoG04]. The circuit consists of four D-flip flops. The FD flip-flop has inputs CLK0 and CLK1 and outputs a signal S0r which is used as the clock input signal to the FDCE flip-flop and the FDE flip-flop. If CLK1 samples CLK0

while CLK0 has a low signal, the S0r output will be low. If CLK1 samples CLK0 while CLK0 has a high signal the S0r output will be high. Figure 9 shows a sample waveform for a rising edge sampling circuit. If CLK1 samples CLK0 in

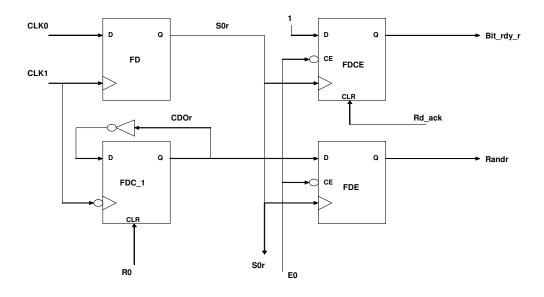


Figure 8. Rising edge sampling circuit [Koh04]

the jitter zone the S0r signal could remain low or change to high on the next rising edge of CLK1 creating an uncertainty region. The signal CDOr is a single bit counter that represents which cycle CLK1 is in (i.e. 0 or 1). The rising edge of S0r captures the cycle of CLK1 and outputs a random bit corresponding to that cycle. If CLK1 samples CLK0 in the jitter zone and CLK0 is high, S0r goes high and captures a high signal on the single bit counter CDOr and the random bit output is a 1. If CLK1 samples CLK0 in the jitter zone and CLK0 is low then S0r does not go high until the next CLK1 cycle which captures a low signal on CDOr and a 0 is output. Thus, the uncertainty region shown in Figure 9 represents the uncertainty of whether CDOr is a 0 or a 1 when the clock is sampled in the jitter zone and S0r goes high.

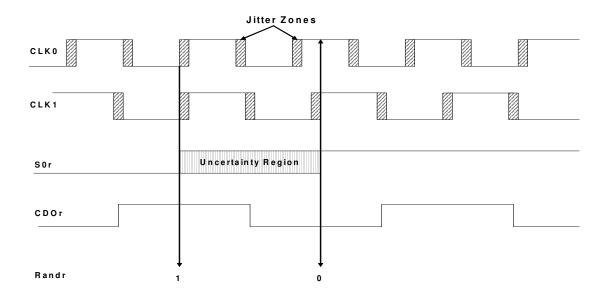


Figure 9. Rising edge sampler circuit with jitter

The S0r signal is also used to notify the control circuit that a new random bit is ready to be output via Bit_rdy_r. The control circuit disables the bit-ready flip-flop (FDCE) and the random output flip-flop (FDE) to avoid any problems with bounce in the S0r signal. If the flip flops were not disabled the circuit could receive multiple S0r edges changing the random bit that is being output if it was captured in the jitter zone [KoG04]. The bit-ready flip-flop is reset when the control circuit has acknowledged that the random bit has been recorded, as is the single bit counter flip-flop (FDC_1) so there is no correlation between consecutive output bits [KoG04]. Once the random bit has been acknowledged the flip-flops are able to receive the next random bit.

The width of the jitter zone is varied, as is the difference in periods between the two oscillators. It is hypothesized that if the difference in periods between the two oscillators is less than or equal to the width of the jitter zone, the output would be a

function of the jitter zone. A sample from the jitter zone is random as it cannot be determined whether a one or a zero would be output. Once the difference in periods between the two oscillators is greater than the width of the jitter zone, the output bits should no longer be random because many of the samples taken would then be deterministic.

4.3.1 Results of Rising Edge Sampling

Data for a 24 ps jitter zone was originally collected for oscillators with a difference of 10 ps, 22 ps, 34 ps, 50 ps and 80 ps based on the hypothesis that once the difference in periods was greater than the length of the jitter zone, the numbers would no longer be random. Additional data was collected at greater period differences after all the original data resulted in random outputs. The difference in periods was increased until the proportion of p-values greater than or equal to 0.01, was less than 0.895607 for more than two of the NIST tests performed. The period difference was increased again to validate that the generator output would still fail to produce a random output based on the criteria set in the previous section. Table 3 shows the proportion of sequences that passed the NIST tests performed on the bits produced by the random number generator in the simulation. The proportion value must be 0.895607 or greater to be considered a random sequence for a sample size of ten sequences. All NIST tests, for this particular set of binary sequences, with a failing proportion are highlighted in dark grey. Any test resulting in a proportion of 0.9 is highlighted in light grey. The small sample size that results in a proportion of 0.9 (0.89 is the minimum for being considered random) should undergo further testing with a larger sample size to determine if the passing proportion

value continues to hold. The non-periodic template matching test resulted in 148 proportions. The tables in this section show the fraction of non-periodic tests that had a proportion of 0.9 or greater. The individual proportions for the 148 non-periodic template matching tests performed are available in Appendix A.

Table 3. Proportions for NIST test run on debiased data for oscillators with period differences of 50 ps, 100 ps, 120 ps, 140 ps, 160 ps with a 24 ps jitter zone sampled on the rising edge.

	6 · ·	Pro	oportion	ı s- 24 ps	jitter Ri	sing edg	e sampli	ng(XOR	ed)	
	50	ps	100 ps		120 ps		140 ps		160 ps	
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2
frequency block	1.00	1.00	1.00	1.00	0.90	1.00	0.00	0.10	0.90	0.80
frequency cumulative-	1.00	1.00	1.00	0.90	1.00	1.00	0.50	0.90	1.00	1.00
sums cumulative-	1.00	1.00	1.00	1.00	1.00	1.00	0.00	0.10	0.90	0.80
sums	1.00	1.00	1.00	1.00	0.90	1.00	0.00	0.10	0.90	0.80
runs	1.00	1.00	1.00	1.00	1.00	1.00	0.50	0.50	1.00	1.00
fft	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
non										
periodic*	0.99	0.97	0.95	0.97	0.98	1.00	0.99	0.95	0.99	0.96
aspen	1.00	1.00	0.90	1.00	1.00	1.00	1.00	0.90	1.00	1.00
serial	1.00	1.00	0.90	1.00	1.00	1.00	1.00	1.00	1.00	1.00
serial	1.00	1.00	1.00	1.00	1.00	0.90	1.00	1.00	1.00	1.00

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

The random number generator, with a 24 ps jitter zone in the oscillators, fails to produce random output in this simulation when the difference in the oscillator frequency increases from 120 ps to 140 ps. The failure occurs when the frequency difference is between five times the width of the jitter zone (24 ps x 5=120 ps) and approximately six times the width of the jitter zone (24 ps x 5.8=139 ps) which is significantly more than hypothesized.

Table 4. Proportions for NIST test run on debiased data for oscillators with period differences of 250 ps, 300 ps, 320 ps, 350 ps, 436 ps, with a 70 ps jitter zone, sampled on the rising edge

		Proportion 70 ps jitter Rising edge sampling(XORed)												
	250) ps	300) ps	320) ps	350 ps		436 ps					
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2				
frequency	1.00	1.00	0.90	1.00	0.20	0.00	0.00	0.00	0.00	0.00				
block														
frequency	0.90	1.00	1.00	1.00	0.70	0.70	0.20	0.00	0.00	0.00				
cumulative-							0.00		0.00					
sums	1.00	1.00	0.90	1.00	0.20	0.00	0.00	_ 0.00 _	0.00	0.00				
cumulative-	0.90	0.90	0.90	1.00	0.20	0.00	0.00	0.00	0.00	0.00				
sums														
runs	1.00	1.00	1.00	1.00	0.40	0.40	0.00	0.00	0.00	0.00				
fft	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00				
non														
periodic *	0.97	0.98	0.98	0.99	0.99	0.95	0.93	0.93	0.89	0.88				
aspen	1.00	1.00	1.00	1.00	1.00	0.80	0.80	0.70	0.00	0.00				
serial	1.00	1.00	1.00	1.00	1.00	1.00	0.80	0.80	0.00	0.00				
serial	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.60				

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

Table 4 shows that a random number generator with oscillators having a 70 ps jitter zone fails to produce random outputs when the difference of frequency is between 300 ps and 320 ps. The failure to produce a random output fall between 4.3 times the width of the jitter zone (70 ps x 4.3 = 301 ps) and 4.6 times the width of the jitter zone (70 ps x 4.6 = 322 ps). Note that the multiplicative value of the jitter has decreased from the values observed in a generator having oscillators with a 24 ps jitter zone.

Table 5 and Table 6 are the proportion results for generators with oscillators having a 140 ps jitter zone and a 200 ps jitter zone respectively. The test set in Table 5 shows that a generator with a 140 ps jitter zone will stop producing a random output when difference in periods of the two oscillators is between 436 ps and 486 ps or 3.1

times the width of the jitter zone (140 ps x 3.1 = 434 ps) and 3.5 times the width of the jitter zone (140 ps x 3.5 = 490 ps). Oscillators with a jitter zone of 200 ps stop producing random bits when the difference in the period is between 586 ps (200 ps x 2.9 = 580 ps) and 630 ps (200 ps x 3.2 = 640 ps). All of the jitter zones widths and period differences tested with the Fast Fourier Transform (FFT) test had a proportion value of 0.900 or greater indicating there was no periodicity to the output bits [RSN01].

Table 5. Proportions for NIST test run on debiased data for oscillators with period differences of 350 ps, 400 ps, 436 ps, 486 ps, 536 ps with a 140 ps jitter zone, sampled on the rising edge

the mong e	8 -	Proportion 140 ps jitter Rising edge sampling(XORed)											
		Pr	oportio	1 140 ps	jitter Ris	sing edge	e samplir	ng(XORe	ed)				
	350) ps	400) ps	436	s ps	486 ps		536 ps				
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2			
frequency	0.90	1.00	1.00	1.00	0.90	1.00	0.00	0.20	0.00	0.00			
block													
frequency	1.00	1.00	1.00	1.00	1.00	1.00	0.40	0.70	0.00	0.00			
cumulative-													
sums	0.90	1.00	1.00	1.00	0.90	1.00	0.00	0.20	0.00	0.00			
cumulative-													
sums	0.90	1.00	1.00	1.00	0.90	1.00	0.00	0.20	0.00	0.00			
runs	1.00	1.00	1.00	1.00	1.00	1.00	0.20	0.60	0.00	0.00			
fft	1.00	1.00	0.90	1.00	1.00	1.00	1.00	1.00	1.00	1.00			
non													
periodic *	0.93	0.97	0.98	0.98	0.98	0.97	0.97	0.99	0.96	0.97			
aspen	1.00	1.00	1.00	1.00	1.00	0.90	0.90	1.00	0.80	0.50			
serial	1.00	1.00	1.00	1.00	1.00	1.00	0.90	1.00	0.90	0.90			
serial	1.00	1.00	1.00	1.00	1.00	0.80	1.00	1.00	1.00	1.00			

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

Table 6. Proportions for NIST test run on debiased data for oscillators with period differences of 436 ps, 486 ps, 536 ps, 586 ps, 630 ps with a 200 ps jitter zone sampled on the rising edge

38		Pr	oportio	1 2 0 0 ps	jitter Ris	sing edge	e samplir	ng(XORe	ed)	
	436	s ps	486	s ps	536	536 ps		586 ps) ps
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2
frequency	1.00	1.00	1.00	1.00	0.90	1.00	0.90	1.00	0.00	0.00
block										
frequency	0.90	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.60	_ 0.00 _
cumulative-	4.00	0.00	4.00	0.00	0.00	4.00	0.00	4.00	0.40	0.00
sums	1.00	0.90	1.00	0.90	0.90	1.00	0.90	1.00	0.10	0.00
cumulative-	1.00	1.00	1.00	1.00	0.90	1.00	0.90	0.90	0.10	0.00
sums	1.00	1.00	1.00	1.00	1.00	0.90	1.00	1.00	0.10	0.00
runs fft	1.00	1.00	1.00	1.00	0.90	1.00	0.90	1.00	1.00	1.00
_	1.00	1.00	1.00	1.00	0.90	1.00	0.90	1.00	1.00	1.00
non periodic	0.99	0.98	0.99	0.98	0.98	0.97	0.97	0.97	0.98	0.82
aspen	1.00	0.90	1.00	0.90	1.00	0.90	1.00	1.00	0.90	0.02
serial	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.00
serial	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

4.3.2 Analysis of rising edge sampling

The simulated random number generator produced random outputs for a particular width of a jitter zone. The point at which the output becomes non-random appears to be proportionally related to the oscillator period differences and the jitter zone width.

Figure 10 shows CLK0 and CLK1 with the same jitter zone width. If the jitter zones just barely overlap, then the sample can take place anywhere up to 2x the width of the jitter zone (48 ps for a 24 ps jitter zone and 140 ps for a 70 ps jitter zone) and still be considered non-deterministic. The TRNG output remains random for more than 2x the width of the jitter zone because every output bit does not need to be non-deterministic. For the output to be random only the majority of the captured bits need to be non-deterministic allowing for greater frequency differences between the two oscillators.

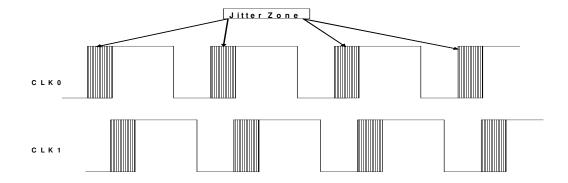


Figure 10. Jitter zone

Table 7 and 8 show the individual jitter zones of the two clock oscillators when S0r goes high and captures the output bit of the generator. The clock cycles examined for a particular instance of S0r going high are grouped together and denoted by the shading or lack of shading in the rows. The first column labels, clk0 or clk1, identify the signal for the data in the corresponding row. The second column is the timing of the jitter zone range for a particular cycle of the oscillator. The third column records whether the output bit is deterministic or non-deterministic. The oscillator rising clock edge can happen at any point in the jitter zone range. The clock cycle where S0r goes high and the output bit is captured is examined to see if the jitter zones of the oscillators overlap. If jitter zones do not overlap then the jitter zone of the previous cycle is examined. If either of the jitter zones overlap then the output bit could be a one or a zero and is non-deterministic. The previous cycle of the oscillator jitter zones is examined because the jitter zones may have overlapped in the previous cycle capturing a low random bit (Figure 9). The output bit is a non-deterministic bit if the jitter zones of the two clocks overlap during one of the two clock oscillator cycles. If the jitter zones of the two clock cycles do not overlap when the

output bit is captured or in the previous cycle then the bit is considered a deterministic bit.

Table 7. Jitter zone ranges for clock edges when capturing an output bit for clocks with a 70 ps jitter zone and period difference between the clocks of 300 ps.

	Jitter Zone Range	Output from RNG
clk0	184.940-185.010ns	
clk1	184.823-184.893ns	deterministic
clk0	192.364-192.434ns	deterministic
clk1	192.534-192.604ns	
clk0	370.020-370.090ns	
clk1	369.784-369.854ns	deterministic
clk0	377.429-377.498ns	deterministic
clk1	377.526-377.596ns	
clk0	570.249-570.319ns	non-deterministic
clk1	570.251-570.321ns	non-deterministic
clk0	762.833-762.903ns	non deterministic
clk1	762.816-762.886ns	mon-deterministic
clk0	955.408-955.478ns	deteministic
clk1	955.548-955.618ns	deterministic
clk0	1140.552-1140.622ns	non-deterministic
clk1	1140.583-1140.653ns	non-deterministic
clk0	1325.531-1325.601ns	non deterministics
clk1	1325.557-1325.627ns	non-deterministics
clk0	1510.714-1510.784ns	non deterministic
clk1	1510.698-1510.768ns	non-deterministic
clk0	1710.963-1711.021ns	non deterministic
clk1	1710.984-1711.054ns	non-deterministic
clk0	1903.704-1903.774ns	non deterministic
clk1	1903.649-1903.719ns	non-deterministic
clk0	2096.338-2096.408ns	
clk1	2096.254-2096.324ns	datarministia
clk0	2103.720-2103.790ns	deterministic
clk1	2103.909-2103.979ns	
clk0	2288.915-2288.985ns	non deterministic
clk1	2287.849-2287.919ns	non-deterministic
clk0	2489.197-2489.267ns	dotomorioistis
clk1	2489.324-2489.394ns	deterministic
clk0	2681.812-2681.882ns	non determinists
clk1	2681.797-2681.867ns	non-deterministic
clk0	2882.061-2882.131ns	non deterministic
clk1	2882.120-2882.172ns	non-deterministic
clk0	3059.685-3059.755ns	
clk1	3059.665-3059.725ns	non-deterministic

The jitter zone range is computed using the timing of the clock oscillators falling edge and adding to it the range of time that the clock signal could go high. CLK0 is the base clock and has a frequency of 135 MHz. The time period for one cycle is 7.408 ns. A half cycle will average 3.704 ns and with a 70 ps jitter zone the half cycle would be between 3.669 ps and 3.739 ps. The clock observations in Table 7 are for a clock oscillator with a 300 ps difference in the periods, therefore CLK1 rising edge could occur between 3.819 ns and 3.889 ns after the previous falling edge of the clock.

$$half _cycle = 3.704ns + \frac{T \pm J}{2} \tag{4}$$

Thus, the jitter zone range is where T is the difference between the two clock oscillators periods and J is the width of the jitter zone.

A period difference of 300 ps and jitter zone of 70 ps results in a majority of the bits being non-deterministic bits (Table 7) and the statistical tests run on the data conclude the output from the generator is random. Table 8 shows the jitter zone ranges for clock oscillators with a 70 ps jitter zone and difference in clock periods of 350 ps. The output of the random number generator appears to produce more deterministic bits than non-deterministic bits for the first set of bits output. More deterministic bits than non-deterministic bits give a binary sequence of bits that does not pass NIST tests.

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Table 8. Jitter zone ranges for clock edges when capturing an output bit for clocks with a 70 ps jitter zone and period difference between the clocks of 350 ps.

	Jitter Zone Range	Output from RNG
clk0	170.494-170.564ns	
clk1	170.543-170.613ns	non-deterministic
clk0	340.923-340.993ns	
clk1	341.068-341.138ns	deterministic
clk0	503.935-504.005ns	
clk1	504.074-504.114ns	deterministic
clk0	659.263-659.333ns	
clk1	659.238-659.308ns	non-deterministic
clk0	822.104-822.174ns	data marinistia
clk1	822.006-822.076ns	deterministic
clk0	985.102-985.172ns	
clk1	984.967-985.037ns	deterministic
clk0	992.497-992.567ns	deterministic
clk1	992.709-992.779ns	
clk0	1148.026-1148.096ns	
clk1	1147.92-1147.99ns	deterministic
clk0	1155.435-1155.505ns	deterministic
clk1	1155.724-1155.794ns	
clk0	1310.993-1311.063ns	non-deterministic
clk1	1311.006-1311.076ns	non-deterministic
clk0	1474.118-1474.188ns	non-deterministic
clk1	1474.058-1474.128ns	Hon-deterministic
clk0	1641.024-1644.763ns	deterministic
clk1	1640.983-1644.897ns	Geterminatio

As the jitter zone gets larger, a smaller proportion of difference in periods is needed for a sequence of bits to remain random. A jitter zone of 200 ps produced a non-random sequence of bits between 2.0 and 3.0 times the width of the jitter zone. A jitter zone of 140 ps produced non-random sequence of bits between 3.1 and 3.5 times the width of the jitter zone. The oscillator with a jitter zone of 70 ps produced a non-random sequence of bits when the difference in period between the two oscillators was about 4.5

times the width of the jitter zone while oscillators with a 24 ps jitter zone did not fail until the two oscillators had a difference in frequency of almost 6 times the width of the jitter zone.

4.4 Rising and Falling Edge Sampling

Rising and falling edge sampling use the same two clock oscillators and sends the signals into two similar sampling circuits. One sampling circuit uses the rising edge of CLK1 to sample CLK0 (Figure 8) and the other circuit uses the falling edge of CLK1 to sample CLK0 (Figure 11). The clock edge on which the single bit counter changes states also had to be changed to rising edge so the single bit counter and the S0f signals would not change states at the same instance. The bits from each of the individual samplers were checked and were both random for the same oscillator period differences that tested random in rising edge only sampling list. The outputs of the two sampler circuits were then combined to form a single output. Figure 12 is a sample waveform from the rising and falling edge sampling circuit. The single output alternates between a rising edge sampled bit and a falling edge sampled bit giving an bit output rate of almost twice the rate of sampling on the rising edge only. If either bit_rdy_r or bit_rdy_f goes high, a signal that a random bit is ready is sent to the control circuit. If bit_rdy_r goes high then randr is the random bit. If bit_rdy_f goes high then rand_f is the random bit.

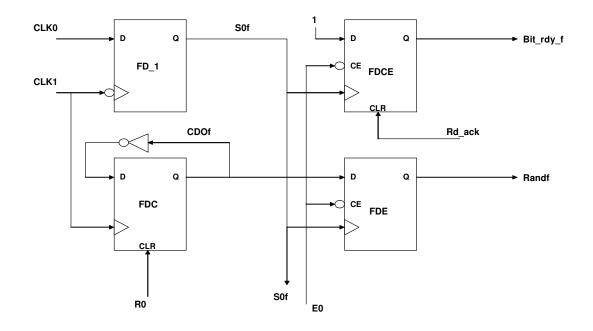


Figure 11. Falling edge sampling circuit

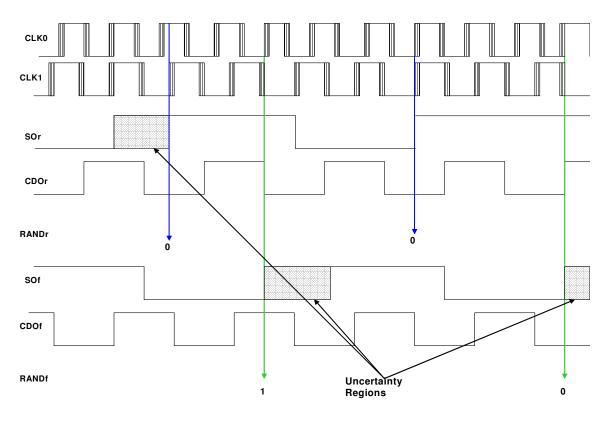


Figure 12. Rising and falling edge sampling circuit (signals with jitter)

4.4.1 Results of Rising and Falling Edge Sampling

The results of the NIST test for the random number generator for data gathered on the rising and falling edges are shown below in Tables 9 to 12.

Table 9. Proportions for NIST test run on debiased data for oscillators with period differences of 50 ps, 100 ps, 120 ps, 140 ps, 160 ps with a 24 ps jitter zone, sampled on the rising and falling edge.

	F	Proportions- 24 ps jitter Rising and falling edge sampling(XORed)											
	50	ps	100) ps	120) ps	140 ps		160) ps			
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2			
frequency	1.00	1.00	1.00	1.00	0.40	0.90	0.00	0.00	0.00	0.00			
block													
frequency	1.00	1.00	1.00	1.00	0.90	1.00	0.00	0.00	0.00	0.00			
cumulative-													
sums	1.00	1.00	1.00	1.00	0.40	0.90	0.00	0.00	0.00	0.00			
cumulative-													
sums	1.00	1.00	1.00	1.00	0.30	0.80	0.00	_ 0.00 _	_ 0.00 _	0.00			
runs	1.00	1.00	1.00	1.00	0.90	1.00	0.00	0.00	0.00	0.00			
fft	0.90	1.00	1.00	1.00	1.00	0.90	0.90	0.70	0.90	0.90			
non periodic	0.99	0.97	0.99	0.99	0.93	0.97	0.75	0.78	0.91	0.92			
aspen	1.00	1.00	1.00	1.00	1.00	1.00	0.00	0.00	0.00	0.00			
serial	1.00	0.90	1.00	1.00	1.00	1.00	0.00	0.00	0.10	0.30			
serial	0.90	0.90	1.00	1.00	1.00	1.00	0.90	0.90	1.00	0.90			

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

Table 10. Proportions for NIST test run on debiased data for oscillators with period differences of 250 ps, 300 ps, 320 ps, 350 ps, 436 ps, with a 70 ps jitter zone, sampled on the rising and falling edge.

	I	Proporti	on 70 p	s jitter	Rising a	nd falling	g edge s	ampling	(XORed)
	250) ps	300 ps		320	320 ps		350 ps		s ps
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2
frequency block	0.00	_ 0.00 _	0.00	0.00	0.20	0.00	0.00	0.00	_ 0.00 _	0.00
frequency cumulative-	0.00	0.10	0.00	0.00	0.70	0.00	0.00	0.00	0.00	0.00
sums cumulative-	0.00	0.00	0.00	0.00	0.20	0.00	0.00	0.00	0.00	0.00
sums	0.00	0.00	0.00	0.00	0.20	0.00	0.00	0.00	0.00	0.00
runs	0.10	0.00	0.00	0.00	0.40	0.00	0.00	0.00	0.00	0.00
fft	1.00	1.00	1.00	0.90	1.00	0.80	0.00	0.00	0.90	0.90
non periodic										
*	0.94	0.96	0.85	0.89	0.99	0.80	0.77	0.77	0.87	0.86
aspen	0.90	_ 0.50 _	0.10	0.00	1.00	0.00	0.00	0.00	0.00	0.00 _
serial	0.90	0.80	0.20	0.20	1.00	0.00	0.00	0.00	0.00	0.00
serial	0.90	0.90	1.00	1.00	1.00	0.80	0.10	0.50	0.00	0.00

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

Table 11. Proportions for NIST test run on debiased data for oscillators with period differences of 350 ps, 400 ps, 436 ps, 486 ps, 536 ps with a 140 ps jitter zone, sampled on the rising and falling edge.

	Р	Proportion 140 ps jitter Rising and falling edge sampling									
	350) ps	400 ps		436	s ps	486 ps		536	s ps	
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	
frequency	0.10	0.10	0.90	0.80	0.00	0.00	0.00	0.00	0.00	0.00	
block frequency	0.80	0.90	1.00	1.00	0.00	0.00	0.00	0.00	0.00	0.00	
cumulative-sums	0.10	0.10	0.80	0.90	0.00	0.00	0.00	0.00	0.00	0.00	
cumulative-sums	0.10	0.10	0.90	0.80	0.00	0.00	0.00	0.00	0.00	0.00	
runs	0.60	0.40	0.90	1.00	0.00	0.00	0.00	0.00	0.00	0.00	
fft	0.90	1.00	1.00	1.00	1.00	1.00	0.20	0.10	0.90	1.00	
non periodic *	0.99	0.95	0.97	0.99	0.96	0.94	0.77	0.80	0.89	0.92	
aspen	1.00	1.00	1.00	1.00	0.20	0.30	0.00	0.00	0.10	0.00	
serial	1.00	1.00	1.00	1.00	0.50	0.80	0.00	0.00	0.10	0.10	
serial	1.00	1.00	1.00	1.00	1.00	1.00	0.50	0.70	1.00	1.00	

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

Table 12. Proportions for NIST test run on debiased data for oscillators with period differences of 436 ps, 486 ps, 536 ps, 586 ps, 630 ps with a 200 ps jitter zone sampled on the rising edge.

the Hong ed		Proportion 200 ps jitter Rising and falling edge sampling(XORed)										
				<u> </u>								
	436	ps	486 ps		536 ps		586 ps		630 ps			
	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2	trial1	trial2		
frequency	0.60	0.80	0.00	0.00	0.00	0.00	0.40	0.20	0.00	0.10		
block												
frequency	0.90	1.00	0.00	0.00	0.00	0.00	0.80	0.90	0.30	0.60		
cumulative-												
sums	0.60	0.80	0.00	0.00	0.00	0.00	0.50	0.20	0.00	0.10		
cumulative-												
sums	0.60	_ 0.80 _	0.00	0.00	0.00	0.00	0.40	0.30	0.00	0.10		
runs	1.00	1.00	0.00	0.00	0.00	0.00	0.60	0.60	0.10	0.40		
fft	1.00	1.00	1.00	0.90	1.00	1.00	1.00	1.00	1.00	1.00		
non												
periodic	0.97	0.96	0.82	0.82	0.90	0.92	0.95	0.97	0.94	0.98		
aspen	1.00	1.00	0.00	0.00	0.40	0.20	1.00	1.00	0.90	1.00		
serial	1.00	1.00	0.00	0.00	0.40	0.50	1.00	1.00	0.90	1.00		
serial	1.00	1.00	1.00	0.90	1.00	1.00	1.00	1.00	1.00	1.00		

^{*}fraction of non-periodic tests with a proportion of 0.9 or greater

4.4.2 Analysis of Rising and Falling Edge Sampling

The bits produced using both the rising and falling edges of CLK1 appear to be random for a 24 ps jitter and a period difference between the two oscillators of 50 ps and 100 ps. The output is not random for one set of data with a period difference of 120 ps and yet is random for the other set of data. Once the difference in periods is greater than 120 ps, the output of the generator is no longer random. The output of the random number generator does not appear to be random for any of the larger jitter zones at period differences that were tested except for a jitter zone of 140 ps with a period difference of 400 ps. Additional data would confirm whether the results hold for a larger sample size.

There appears to be a correlation between the rising edge bits and falling edge bits. Independently, the rising edge bits were random at the smaller period differences as were the falling edge bits. Once the samples were put together to form a single output the stream of data was no longer random.

4.5 Summary

A cryptographically secure random number generator is possible in a field programmable gate array using two oscillators at very small period differences using the sampling circuit of Kohlbrenner [Koh04]. This circuit was taken a step further in this research to determine the limitations of the jitter zone and period differences which still result in a random output. This research also incorporated the technique of sampling on both the rising edge of the oscillator and the falling edge of the oscillator.

For rising edge sampling, the output is not random as the difference in periods becomes large compared to the width of the jitter zone. The failure point relative to the

width of the jitter zone divided by the difference in period seems to decrease. It is unknown why the multiplicative factor of the jitter zone decreases as the width of the jitter zone increases. Even so, the results show sampling on the rising and falling edge of the oscillator does produce a random output if the width of the jitter zone and the difference in period in the oscillators is small.

There are limitations in producing random output from the generator used.

Further research could determine if these results will continue to hold true for multiple data sets. Additional data would allow multiple data sets to be tested as well as enough data to run all fifteen available NIST tests. The pseudo number generator used for simulating the jitter in the oscillators may play a role in the point of failure observed.

Jitter is a difficult phenomenon to simulate, therefore prior to implementation in a production system, additional testing they should be done in hardware.

V. Conclusions and Recommendations

5.1 Overview

A true random number generator (TRNG) can be implemented in a Field Programmable Gate array for cryptographic applications using the jitter on a signal and an oscillator sampling technique [Koh04]. This research expands Kohlbrenner's work by identifying three limitations of that technique.

5.2 Conclusion

The limitations identified include the amount of jitter in the clock oscillators for the TRNG to be random, the difference in periods between the two sampling oscillators, and the whether the speed of the generator can be increased by sampling on the rising and falling edge of the oscillator signal.

There is a correlation between the amount of jitter present and the allowable difference in periods for a TRNG. A TRNG with two clock oscillators, one with a base frequency of 135 MHz, and a 24 ps jitter zone, sampling on the rising edge, will output random bits as long as the difference in periods between the two oscillators is 120 ps or less (24/120=0.2). As the jitter zone gets larger, the proportion of the jitter zone to the difference in periods must increase for the output to remain random (70/300=0.233, 140/436=0.321, 200/586=0.341).

Trying to speed up the output of the TRNG by sampling the oscillator on the rising and falling edge was not effective. A random sequence was output only when the jitter zone was 24 ps and the difference in periods was 50 ps and 100 ps. A larger difference in periods produced consecutive output bits that were correlated.

5.3 Future Research

Further research into the TRNG in a FPGA should include generating larger data samples so all NIST tests can be run on the generator output. Testing additional jitter zone widths and differences in periods should also be done and an algorithm developed that can determine the maximum frequency difference between two oscillators for a particular jitter zone. A base frequency of a 135 MHz was used in this research for the oscillators with a system clock of 50 MHz. Additional research would include larger and smaller base frequencies and faster system clocks.

Sampling using both the rising and falling edge of the oscillator is a simple way to speed up the output from the system. Research to determine how to combine the rising and falling samples at particular frequencies so the output remains random is needed.

Once the specific limitations are determined, built in self tests need to be included in the VHDL code to assure the systems outputs remain random. The system should be implemented and tested on several different types of FPGA boards. Things to consider when placing the system on a board is whether the difference in periods becomes greater or smaller based on distance of the placement of the oscillators. The heat of the board over time should also be considered as it can affect the frequency of the oscillators.

Appendix A

FinalAnalysisReport from NIST

Report for all test run with oscillators with a 24 ps jitter zone. Final Analysis Report for 70 ps, 140 ps, and 200 ps available of CD Rom.

10nsc_50psf_24jrout_lq_XORed.txt

(10ns system clk $\frac{1}{2}$ cycle, 50 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets 1 through q and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	С6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
0	0	0	2	0	2	2	1	2	1	0.534146	1.0000	frequency
3	0	1	1	1	0	0	4	0	0	0.035174	1.0000	block-frequency
0	0	1	1	1	0	4	3	0	0	0.035174	1.0000	cumulative-sums
0	0	0	0	1	2	0	3	2	2	0.213309	1.0000	cumulative-sums
1	2	1	0	0	1	1	2	1	1	0.911413	1.0000	runs
2	2	1	2	0	0	2	1	0	0	0.534146	1.0000	fft
3	2	1	0	0	0	2	1	0	1	0.350485	0.9000 *	nonperiodic-templates
0	0	2	3	0	1	2	0	2	0	0.213309	1.0000	nonperiodic-templates
2	0	0	0	2	0	1	1	1	3	0.350485	1.0000	nonperiodic-templates
1	1	1	0	1	2	0	2	2	0	0.739918	1.0000	nonperiodic-templates
1	0	1	1	1	0	2	2	1	1	0.911413	1.0000	nonperiodic-templates
4	0	0	1	2	0	0	2	1	0	0.066882	0.9000 *	nonperiodic-templates
0	2	0	0	1	2	1	1	1	2	0.739918	1.0000	nonperiodic-templates
0	0	4	0	2	2	0	1	1	0	0.066882	1.0000	nonperiodic-templates
1	0	3	0	1	1	1	2	1	0	0.534146	1.0000	nonperiodic-templates
0	0	3	0	1	1	2	0	1	2	0.350485	1.0000	nonperiodic-templates
0	3	1	1	4	1	0	0	0	0	0.035174	1.0000	nonperiodic-templates
2	0	0	0	1	1	2	2	1	1	0.739918	1.0000	nonperiodic-templates
2	1	1	0	1	0	1	0	2	2	0.739918	0.9000 *	nonperiodic-templates
1	0	0	0	2	0	1	2	3	1	0.350485	1.0000	nonperiodic-templates
0	1	1	1	0	0	3	1	0	3	0.213309	1.0000	nonperiodic-templates
2	1	1	0	0	1	2	1	2	0	0.739918	1.0000	nonperiodic-templates
0	1	0	0	2	1	1	2	1	2	0.739918	1.0000	nonperiodic-templates
3	1	0	1	1	1	1	0	1	1	0.739918	1.0000	nonperiodic-templates
1	0	1	3	1	1	2	0	0	1	0.534146	1.0000	nonperiodic-templates
2	2	0	0	3	0	1	0	2	0	0.213309	0.9000 *	nonperiodic-templates
3	0	2	0	0	0	2	1	0	2	0.213309	0.9000 *	nonperiodic-templates
1	2	1	0	1	3	0	0	1	1	0.534146	1.0000	nonperiodic-templates
1	0	0	0	0	0	2	0	4	3	0.017912	1.0000	nonperiodic-templates
2	0	0	1	4	1	1	0	1	0	0.122325	1.0000	nonperiodic-templates
0	1	0	0	0	2	1	1	1	4	0.122325	1.0000	nonperiodic-templates
0	0	2	1	1	0	1	2	1	2	0.739918	1.0000	nonperiodic-templates
1	2	0	0	3	1	0	1	1	1	0.534146	1.0000	nonperiodic-templates
0	1	0	1	1	0	1	2	2	2	0.739918	1.0000	nonperiodic-templates
1	1	1	2	0	1	1	1	2	0	0.911413	1.0000	nonperiodic-templates
0	1	0	0	0	1	4	0	1	3	0.035174	1.0000	nonperiodic-templates
1	0	1	0	0	0	3	3	1	1	0.213309	1.0000	nonperiodic-templates
1	0	1	0	0	1	2	1	0	4	0.122325	1.0000	nonperiodic-templates
0	1	1	1	1	1	1	2	0	2	0.911413	1.0000	nonperiodic-templates
1	2	2	0	1	3	0	1	0	0	0.350485	0.9000 *	nonperiodic-templates
0	1	0	1	1	2	1	1	3	0	0.534146	1.0000	nonperiodic-templates
1	1	1	0	0	1	1	1	1	3	0.739918	0.9000 *	nonperiodic-templates
0	1	1	3	1	2	0	1	0	1	0.534146	1.0000	nonperiodic-templates

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1	2	1	3	1	1	1	0	0	0	0.534146	1.0000	nonperiodic-templates
0	0	1	1	1	1	1	2	3	0	0.534146	1.0000	nonperiodic-templates
1	1	1	1	1	1	2	1	0	1	0.991468	1.0000	nonperiodic-templates
0	1	1	0	1	1	2	1	2	1	0.911413	1.0000	nonperiodic-templates
1	0	0	0	1	4	0	1	1	2	0.122325	1.0000	nonperiodic-templates
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1	0	2	2	1	0	0	4	0	0	0.066882	0.9000 *	nonperiodic-templates
2	0	0	0	2	0	1	1	0	4	0.066882	1.0000	nonperiodic-templates
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1	1	2	2	0	2	0	0	1	1	0.739918	0.9000 *	nonperiodic-templates
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1	1	1	0	0	2	1	2	1	1	0.911413	0.9000 *	nonperiodic-templates
0	1	1	1	1	1	1	1	2	1	0.991468	1.0000	nonperiodic-templates
0	0	3	2	1	0	2	0	1	1	0.350485	1.0000	nonperiodic-templates
0	2	1	0	1	0	1	2	2	1	0.739918	1.0000	nonperiodic-templates
0	1	3	1	0	1	0	0	1	3	0.213309	1.0000	nonperiodic-templates
0	2	1	0	1	2	1	2	1	0	0.739918	1.0000	nonperiodic-templates
3	2	1	0	0	0	2	1	0	1	0.350485	0.9000 *	nonperiodic-templates
2	0	2	1	0	1	0	3	0	1	0.350485	1.0000	nonperiodic-templates
3	0	2	1	1	1	0	1	1	0	0.534146	0.9000 *	nonperiodic-templates
0	0	0	0	1	3	2	1	2	1	0.350485	1.0000	nonperiodic-templates
1	1	0	0	2	2	1	1	0	2	0.739918	1.0000	nonperiodic-templates
0	0	4	1	1	1	1	1	1	0	0.213309	1.0000	nonperiodic-templates
1	2	3	0	0	0	1	1	0	2	0.350485	1.0000	apen
2	1	1	3	1	1	0	0	0	1	0.534146	1.0000	serial
3	1	1	1	1	2	0	1	0	0	0.534146	1.0000	serial

The minimum pass rate for each statistical test with the exception of the random excursion (variant) test is approximately = 0.895607 for a sample size = 10 binary sequences.

For further guidelines construct a probability table using the MAPLE program provided in the addendum section of the documentation.

50psf_24jrout_rvX_FAR

(10ns system clk $\frac{1}{2}$ cycle, 50 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets r through v and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

O													
O	C1	C2 	C3	C4	C5	C6	C7	C8	C9	C10 	P-VALUE	PROPORTION	STATISTICAL TEST
O													
0													
1													
1													
1													
1													
0													
0													=
2 0 2 2 1 1 1 0 0 0 1 1 0.739918 1.0000 nonperiodic-templates nonp													
0 3 0 0 0 2 1 1 1 1 1 1 0 .534146 1.0000 nonperiodic-templates 0 2 1 1 3 3 0 1 2 0 0 0 .350485 1.0000 nonperiodic-templates 0 2 1 1 1 3 0 1 1 2 0 0 0 0.350485 1.0000 nonperiodic-templates 1 0 0 1 1 3 1 0 0 0 2 2 0.534146 1.0000 nonperiodic-templates 1 0 0 1 1 3 1 0 0 0 2 2 1 0.739918 1.0000 nonperiodic-templates 1 0 1 1 0 2 1 2 0 0 2 1 0.739918 1.0000 nonperiodic-templates 1 1 0 1 1 0 2 1 1 2 1 0.911413 1.0000 nonperiodic-templates 1 1 0 1 1 0 2 1 1 2 1 0.911413 1.0000 nonperiodic-templates 1 1 0 1 1 0 2 1 1 2 1 0.911413 1.0000 nonperiodic-templates 1 1 0 1 1 0 2 1 1 2 1 0.911413 1.0000 nonperiodic-templates 1 1 0 1 1 0 2 1 1 2 0 0.534146 1.0000 nonperiodic-templates 2 0 2 2 0 1 1 0 3 0 0 0.213309 1.0000 nonperiodic-templates 3 0 1 1 1 1 0 0 2 1 1 1 0.534146 1.0000 nonperiodic-templates 3 0 1 1 1 1 0 0 2 2 1 1 0.534146 1.0000 nonperiodic-templates 1 1 0 0 1 2 0 0 0.350485 1.0000 nonperiodic-templates 1 1 1 0 0 0 2 2 1 1 1 0.534146 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 2 2 1 1 1 0.931413 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 2 2 1 1 1 0.931448 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 2 2 1 1 1 0.931448 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 2 2 1 1 1 0.931448 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 0 2 2 0 1 1 1 0.931448 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 2 0 0 1 2 1 1 1 0.931448 1.0000 nonperiodic-templates 1 1 1 1 1 1 0 2 2 0 1 1 1 0.93448 1.0000 nonperiodic-templates 1 1 1 1 1 0 1 2 0 0 1 1 2 0.534146 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 2 2 0 0 0.350485 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 0 2 1 1 1 0.9354146 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 2 1 1 1 0.9354146 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 0 1 1 0.334146 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 0 0 0 0 0.350485 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 0 0 0 0 0.350485 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2	0	2	2	1	1	0	0	1				
2	2	0	0	1	0	3	0	2	2	0	0.213309	1.0000	nonperiodic-templates
O	0	3		0	2	1		1	1	1	0.534146	1.0000	nonperiodic-templates
2 2 1 1 1 0 1 1 2 2 0 0 0.739918 1.0000 nonperiodic-templates 1 0 0 1 3 1 0 0 2 2 0.350485 1.0000 nonperiodic-templates 0 1 1 0 0 2 1 2 0 0 2 1 0.739918 1.0000 nonperiodic-templates 0 1 1 0 0 2 1 1 2 0 2 1 0.739918 1.0000 nonperiodic-templates 1 1 0 1 1 0 2 1 1 2 0 2 1 1 0.911413 1.0000 nonperiodic-templates 0 1 1 1 1 2 3 1 1 1 0 0 0.534146 1.0000 nonperiodic-templates 0 1 1 1 1 2 3 1 1 1 0 0 0.534146 1.0000 nonperiodic-templates 0 1 1 1 1 2 3 1 1 1 0 0 0.534146 1.0000 nonperiodic-templates 0 1 1 1 0 2 0 1 3 1 0.534146 1.0000 nonperiodic-templates 1 0 1 1 0 2 2 0 1 3 1 0.534146 1.0000 nonperiodic-templates 0 1 1 1 1 0 0 2 0 1 3 1 0.534146 1.0000 nonperiodic-templates 0 1 4 1 1 0 0 1 2 0 0 0.350485 1.0000 nonperiodic-templates 0 1 4 1 1 1 0 1 2 0 0 0.350485 1.0000 nonperiodic-templates 1 1 1 0 0 0 2 2 1 1 1 0.991468 1.0000 nonperiodic-templates 1 1 1 1 1 1 0 2 2 1 1 0.9534146 1.0000 nonperiodic-templates 1 3 1 0 1 2 0 1 1 0 0.534146 1.0000 nonperiodic-templates 0 1 1 1 3 1 0 1 2 0 1 1 0.534146 1.0000 nonperiodic-templates 0 1 1 1 3 1 0 1 2 0 1 1 0.534146 1.0000 nonperiodic-templates 1 1 1 1 1 1 0 2 2 0 0 0.739918 1.0000 nonperiodic-templates 0 1 1 1 3 1 0 0 1 2 0 0 1 1 0.534146 1.0000 nonperiodic-templates 1 1 1 0 0 0 2 1 1 1 1 2 1 0.931413 0.0000 nonperiodic-templates 1 1 1 0 0 0 2 1 1 1 1 2 0 0.350485 1.0000 nonperiodic-templates 1 1 1 0 0 0 0 2 1 1 1 1 2 0 0.330485 1.0000 nonperiodic-templates 1 1 1 1 0 0 2 0 0 1 0 0.350485 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 0 0 4 0 3 0.035174 0.9000 * nonperiodic-templates 1 1 1 1 0 0 0 0 3 1 1 0.033446 1.0000 nonperiodic-templates 1 1 1 1 0 0 0 0 3 1 1 0.033446 1.0000 nonperiodic-templates 1 1 1 1 1 1 2 2 0 2 0 0.330485 1.0000 nonperiodic-templates 1 1 1 1 1 1 2 1 0 0 1 0 0.350485 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 0 0 0 4 0 0 0.330485 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 1 2 2 1 0 0 1 0 0.350485 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 1 2 2 1 0 0 0 0 0 0.350485 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2			0						0		1.0000	
2													
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0 1 1 1 2 2 3 1 1 0 0 0 0.534146 1.0000 nonperiodic-templates 2 0 2 2 0 1 1 0 3 3 0 0 0.213309 1.0000 nonperiodic-templates 3 0 1 1 1 1 0 0 2 0 1 3 1 0.534146 1.0000 nonperiodic-templates 6 1 4 1 1 0 1 2 0 0 0.122325 1.0000 nonperiodic-templates 7 1 0 1 1 0 0 2 2 1 1 0.0534146 1.0000 nonperiodic-templates 8 1 2 0 2 1 3 0 1 0 0 0.350485 1.0000 nonperiodic-templates 9 1 1 1 1 1 1 1 0 2 2 1 0 0.534146 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 1 0 2 2 1 1 0.991468 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 0 2 2 1 1 0.991468 1.0000 nonperiodic-templates 9 1 1 1 3 1 0 1 0 1 2 0.534146 1.0000 nonperiodic-templates 9 1 1 1 1 1 0 0 2 2 1 1 0.534146 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 2 2 0 0 1 1 0.534146 1.0000 nonperiodic-templates 1 1 1 1 0 0 2 2 0 0 1 1 0.22325 1.0000 nonperiodic-templates 1 1 1 1 0 0 2 2 1 1 1 0.2534146 1.0000 nonperiodic-templates 1 1 1 0 0 2 2 1 1 1 0.22325 1.0000 nonperiodic-templates 1 1 1 0 0 2 1 1 1 1 2 1 0.911413 0.9000 *** nonperiodic-templates 1 1 1 0 0 2 1 1 1 1 2 1 0.911413 0.9000 *** nonperiodic-templates 1 1 1 0 0 2 1 1 1 2 0 0.733918 1.0000 nonperiodic-templates 2 1 1 2 0 1 0 1 2 0 0.350485 1.0000 nonperiodic-templates 2 1 1 1 2 0 1 0 1 0 0.3554416 0.8000 *** nonperiodic-templates 1 1 1 0 2 0 0 0 1 0.534146 0.8000 *** nonperiodic-templates 1 1 1 0 1 0 0 0 4 0 0 0.355174 1.0000 nonperiodic-templates 2 0 1 1 1 2 1 1 0 0 0 0.355446 1.0000 nonperiodic-templates 1 0 1 1 0 1 0 0 0 3 1 1 0.213309 1.0000 *** nonperiodic-templates 1 0 1 1 1 0 1 1 0 0 0 0 3 1 1 0.213309 0.9000 *** nonperiodic-templates 1 0 1 1 1 0 0 0 0 3 1 1 0.213309 1.0000 nonperiodic-templates 1 1 1 0 1 0 0 0 2 2 1 1 1 0.08879 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 0 0 0 3 1 1 0.733918 0.9000 *** nonperiodic-templates 1 1 1 1 1 1 0 0 0 0 0.35446 1.0000 nonperiodic-templates 1 1 1 1 1 0 0 0 0 0 3 1 1 0.008879 1.0000 nonperiodic-templates 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1													
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3													
O	3	0	1	1	1	0	0	2	1	1			
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1	0	1	2	1	2	1	1	0	1	0.911413	1.0000	nonperiodic-templates
2	0	1	1	1	1	3	0	1	0	0.534146	1.0000	nonperiodic-templates
0	0	1	2	1	2	0	1	1	2	0.739918	1.0000	nonperiodic-templates
1	1	0	3	2	1	0	0	1	1	0.534146	1.0000	nonperiodic-templates
0	1	0	1	3	1	0	1	2	1	0.534146	1.0000	nonperiodic-templates
1	0	0	0	1	4	1	1	0	2	0.122325	1.0000	nonperiodic-templates
0	0	3	1	1	2	0	3	0	0	0.122325	1.0000	nonperiodic-templates
2	2	0	0	1	2	0	0	3	0	0.213309	1.0000	nonperiodic-templates
1	1	1	3	0	1	1	0	0	2	0.534146	1.0000	nonperiodic-templates
1	2	1	1	1	2	0	1	0	1	0.911413	1.0000	nonperiodic-templates
1	1	0	0	1	3	1	1	2	0	0.534146	1.0000	nonperiodic-templates
0	2	0	0	2	1	2	1	2	0	0.534146	1.0000	nonperiodic-templates
0	1	1	0	1	1	0	2	3	1	0.534146	1.0000	nonperiodic-templates
1	0	1	1	1	0	0	2	4	0	0.122325	0.9000 *	nonperiodic-templates
1	3	2	0	1	2	1	0	0	0	0.350485	1.0000	nonperiodic-templates
0	2	1	0	2	2	2	0	0	1	0.534146	1.0000	nonperiodic-templates
0	0	1	2	1	0	2	0	3	1	0.350485	1.0000	nonperiodic-templates
2	0	1	1	2	0	0	1	2	1	0.739918	1.0000	nonperiodic-templates
2	1	0	2	0	2	1	1	1	0	0.739918	1.0000	nonperiodic-templates
1	1	1	1	1	0	0	3	2	0	0.534146	1.0000	nonperiodic-templates
1	3	1	0	1	1	0	3	0	0	0.213309	1.0000	nonperiodic-templates
0	2	2	0	2	0	1	1	1	1	0.739918	1.0000	nonperiodic-templates
3	0	0	1	1	1	0	2	0	2	0.350485	0.9000 *	nonperiodic-templates
3	2	0	0	1	2	0	2	0	0	0.213309	0.9000 *	nonperiodic-templates
3	2	1	1	0	0	0	3	0	0	0.122325	1.0000	nonperiodic-templates
1	1	0	0	2	0	1	3	1	1	0.534146	1.0000	nonperiodic-templates
2	1	0	2	0	3	0	1	0	1	0.350485	1.0000	apen
1	2	1	1	2	1	0	1	0	1	0.911413	1.0000	serial
0	2	3	0	2	0	2	1	0	0	0.213309	1.0000	serial

The minimum pass rate for each statistical test with the exception of the random excursion (variant) test is approximately = 0.895607 for a sample size = 10 binary sequences.

For further guidelines construct a probability table using the MAPLE program provided in the addendum section of the documentation.

(10ns system clk $\frac{1}{2}$ cycle, 100 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets 1 through q and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
1	0	1	0	2	0	2	2	1	1	0.739918	1.0000	frequency
0	0	1	1	2	3	1	1	0	1	0.534146	1.0000	block-frequency
2	0	0	1	2	1	0	1	1	2	0.739918	1.0000	cumulative-sums
1	0	0	0	1	1	1	2	2	2	0.739918	1.0000	cumulative-sums
2	1	0	0	1	2	2	0	2	0	0.534146	1.0000	runs
0	0	1	0	1	1	2	2	2	1 1	0.739918 0.213309	1.0000	fft nonperiodic-templates
1 2	0	2	0	1	2	0	3	0	0	0.213309	1.0000 0.9000 *	nonperiodic-templates
0	1	1	1	1	0	1	4	1	0	0.213309	1.0000	nonperiodic-templates
0	1	4	1	1	0	0	2	1	0	0.122325	1.0000	nonperiodic-templates
0	1	0	2	1	2	1	2	0	1	0.739918	1.0000	nonperiodic-templates
0	2	2	0	2	1	1	0	1	1	0.739918	1.0000	nonperiodic-templates
0	1	1	2	0	0	2	1	2	1	0.739918	1.0000	nonperiodic-templates
3	2	1	0	1	2	0	0	1	0	0.350485	0.8000 *	nonperiodic-templates
2	0	0	0	4	2	0	0	1	1	0.066882	1.0000	nonperiodic-templates
2	0	0	1	0	3	1	0	1	2	0.350485	1.0000	nonperiodic-templates
1	1	1	2	2	0	0	1	1	1	0.911413	1.0000	nonperiodic-templates
2	0	0	1	1	1	4	0	1	0	0.122325	0.9000 *	nonperiodic-templates
0	1	1	2	4	0	0	0	1	1	0.122325	1.0000	nonperiodic-templates
0	0	0	0 1	2	1 2	1	3	2	1	0.350485	1.0000	nonperiodic-templates nonperiodic-templates
2	0 2	0	0	0	0	1	1 2	0	0	0.350485 0.213309	0.9000 * 0.8000 *	nonperiodic-templates nonperiodic-templates
3	1	0	2	1	1	1	1	0	0	0.534146	0.8000 *	nonperiodic-templates
1	1	0	1	0	2	1	2	1	1	0.911413	0.9000 *	nonperiodic-templates
2	0	1	1	1	2	0	1	2	0	0.739918	0.9000 *	nonperiodic-templates
2	2	0	2	1	1	0	0	1	1	0.739918	1.0000	nonperiodic-templates
2	0	0	2	0	1	2	1	2	0	0.534146	1.0000	nonperiodic-templates
2	0	2	1	0	0	2	2	0	1	0.534146	1.0000	nonperiodic-templates
2	0	2	1	0	2	0	1	2	0	0.534146	0.9000 *	nonperiodic-templates
3	0	1	1	1	1	2	0	0	1	0.534146	0.9000 *	nonperiodic-templates
1	2	2	1	1	2	0	0	0	1	0.739918	1.0000	nonperiodic-templates
1	1	2	0	2	1	1	1	1	0	0.911413	1.0000	nonperiodic-templates
1	1	0	0	1	0	4	1	2	0	0.122325	1.0000	nonperiodic-templates
3	0	1	0 2	1	2	0	1	1	1 2	0.534146	1.0000	nonperiodic-templates
1 3	2	0	1	1 1	2	0	0	1 2	1	0.739918 0.350485	1.0000 0.8000 *	nonperiodic-templates nonperiodic-templates
1	2	1	1	0	1	0	1	3	0	0.534146	0.9000 *	nonperiodic-templates
1	0	3	1	1	1	1	1	1	0	0.739918	0.9000 *	nonperiodic-templates
0	0	1	1	2	0	1	3	2	0	0.350485	1.0000	nonperiodic-templates
0	0	2	1	1	1	1	1	1	2	0.911413	1.0000	nonperiodic-templates
2	0	2	1	1	0	2	0	1	1	0.739918	0.9000 *	nonperiodic-templates
1	4	1	1	1	0	0	0	1	1	0.213309	0.9000 *	nonperiodic-templates
2	2	1	0	1	0	1	0	3	0	0.350485	0.9000 *	nonperiodic-templates
3	0	0	0	1	1	1	1	1	2	0.534146	0.7000 *	nonperiodic-templates
1	1	0	1	2	1	2	1	1	0	0.911413	1.0000	nonperiodic-templates
0	1	2	0	1	2	1	1	1	1	0.911413	1.0000	nonperiodic-templates
1	1	0	0	0	1	1	3	2	1	0.534146	0.9000 *	nonperiodic-templates
3	3	0 2	2	1	1	0	0	0	0	0.122325	1.0000	nonperiodic-templates
1 2	0	1	1 2	1 1	0	1 2	1	0	1	0.911413 0.739918	1.0000	nonperiodic-templates nonperiodic-templates
0	1	1	1	0	5	1	1	0	0	0.739910	1.0000	nonperiodic-templates
2	1	0	3	1	1	1	0	0	1	0.534146	1.0000	nonperiodic-templates
0	3	1	1	2	0	1	1	1	0	0.534146	1.0000	nonperiodic-templates
3	0	0	1	0	0	1	0	4	1	0.035174	1.0000	nonperiodic-templates
0	1	0	1	0	0	2	1	3	2	0.350485	1.0000	nonperiodic-templates
0	0	0	2	2	2	0	0	2	2	0.350485	1.0000	nonperiodic-templates
0	1	2	1	2	0	1	0	3	0	0.350485	1.0000	nonperiodic-templates
1	0	1	2	0	1	0	1	2	2	0.739918	1.0000	nonperiodic-templates

0	1	1	1	0	1	2	2	2	0	0.739918	1 0000		nonnoviodia tomplatos
0	1	2	1	1	0	0	0	3	2	0.759918	1.0000		nonperiodic-templates nonperiodic-templates
1	2	1	0	0	0	2	0	1	3	0.350485	0.9000	*	nonperiodic-templates
0	4	0	0	0	0	2	0	3	1	0.017912	1.0000		nonperiodic-templates
1	0	2	1	1	3	1	1	0	0	0.534146	1.0000		nonperiodic-templates
0	2	1	0	0	2	1	2	1	1	0.739918	1.0000		nonperiodic-templates
3	3	0	1	0	0	2	0	1	0	0.122325	1.0000		nonperiodic-templates
1	3	3	0	0	1	0	0	1	1	0.213309	1.0000		nonperiodic-templates
0	1	1	1	0	0	1	2	2	2	0.739918	1.0000		nonperiodic-templates
0	1	2	1	3	0	1	1	0	1	0.534146	1.0000		nonperiodic-templates
0	1	0	0	0	5	1	0	1	2	0.008879	1.0000		nonperiodic-templates
2	3	0	0	0	0	1	2	0	2	0.213309	0.9000	*	nonperiodic-templates
2	0	1	0	3	0	1	1	2	0	0.350485	1.0000		nonperiodic-templates
0	0	2	0	3	0	0	2	2	1	0.213309	1.0000		nonperiodic-templates
1	3	1	1	0	1	1	1	0	1	0.739918	1.0000		nonperiodic-templates
1 1	1 2	2	0	0	2	0	1	0 1	3 2	0.350485 0.534146	1.0000		nonperiodic-templates
4	1	0	0	2	3	0	0	0	0	0.017912	1.0000	*	nonperiodic-templates nonperiodic-templates
1	1	0	1	0	0	0	4	3	0	0.017912	1.0000		nonperiodic-templates
0	1	0	1	0	2	2	2	2	0	0.534146	1.0000		nonperiodic-templates
0	1	1	0	0	1	1	1	4	1	0.213309	1.0000		nonperiodic-templates
1	0	1	1	1	0	1	1	2	2	0.911413	1.0000		nonperiodic-templates
1	0	1	1	0	0	1	0	4	2	0.122325	1.0000		nonperiodic-templates
1	0	1	0	1	3	1	2	1	0	0.534146	1.0000		nonperiodic-templates
3	1	2	2	0	0	1	1	0	0	0.350485	1.0000		nonperiodic-templates
0	2	0	0	2	3	2	1	0	0	0.213309	1.0000		nonperiodic-templates
3	0	0	1	1	0	1	1	2	1	0.534146	0.8000	*	nonperiodic-templates
0	0	0	1	3	0	3	1	0	2	0.122325	1.0000		nonperiodic-templates
0	1	0	1	2	1	0	1	3	1	0.534146	1.0000		nonperiodic-templates
1	0	1	2	1	0	2	1	1	1	0.911413	1.0000		nonperiodic-templates
1	2	1	0	4	1	0	1	0	0	0.122325	1.0000		nonperiodic-templates
2	1	0	0	1	2	0	2	1	1	0.739918	1.0000		nonperiodic-templates
1	2	2	0	0	1	1	1	2	0	0.739918	1.0000		nonperiodic-templates
2	1	0	1	1	1	2	1	0	1	0.911413	1.0000		nonperiodic-templates
0	2	1	0	2	2	1	0	1	1	0.739918	1.0000		nonperiodic-templates
1	1	2	0	1	3	0	1	1	0	0.534146	1.0000		nonperiodic-templates
1	0	0	1	2	1	0	2	3	0	0.350485	1.0000		nonperiodic-templates
2	1	2	0	0	0	0	0	2	3	0.213309	0.8000	*	nonperiodic-templates
0	2	0	2	1	0	2	2	0	1	0.534146	1.0000		nonperiodic-templates
0	1	1	3	0	0	1	2	1	1	0.534146	1.0000		nonperiodic-templates
0	1	0	1	1	2	0	1	3	1	0.534146	1.0000		nonperiodic-templates
2	2	0	1	1	1	1	1	1	0	0.911413	1.0000		nonperiodic-templates
1	1	0	0	1	2	1	0	1	3	0.534146	0.9000	*	nonperiodic-templates
0	1	0	2	2	2	1	2	0	0	0.534146	1.0000		nonperiodic-templates
1	2	0	2	2	0	0	2	1	0	0.534146		*	nonperiodic-templates
2	2	0	1	1	2	0	0	1	1	0.739918	0.9000	*	nonperiodic-templates
2 1	0	0 2	1 1	2	1	1 1	1 1	2 1	0 1	0.739918	0.8000	^	nonperiodic-templates
3	0 2	1	1	0	0	1	2	0	0	0.911413 0.350485	1.0000		nonperiodic-templates nonperiodic-templates
1	1	3	1	0	1	1	0	2	0		1.0000		
3	0	0	0	2	2	0	0	2	1	0.534146 0.213309	1.0000		nonperiodic-templates nonperiodic-templates
1	1	1	2	0	0	2	0	1	2	0.739918	1.0000		nonperiodic-templates
1	1	1	0	0	1	2	1	2	1	0.735518	1.0000		nonperiodic-templates
0	2	1	2	2	0	1	1	1	0	0.739918	1.0000		nonperiodic-templates
2	0	1	1	2	1	1	0	2	0	0.739918	1.0000		nonperiodic-templates
0	0	3	1	2	1	0	1	1	1	0.534146	1.0000		nonperiodic-templates
1	1	1	0	1	0	4	1	0	1	0.213309	1.0000		nonperiodic-templates
1	0	0	0	1	2	1	3	1	1	0.534146	1.0000		nonperiodic-templates
0	1	0	0	0	0	4	0	3	2	0.017912	1.0000		nonperiodic-templates
1	0	1	2	1	0	1	1	2	1	0.911413	0.9000	*	nonperiodic-templates
0	3	1	0	1	1	0	1	2	1	0.534146	1.0000		nonperiodic-templates
0	1	2	1	0	1	1	1	2	1	0.911413	1.0000		nonperiodic-templates
0	1	2	1	0	1	1	0	3	1	0.534146	1.0000		nonperiodic-templates
2	1	2	1	0	2	2	0	0	0	0.534146	1.0000		nonperiodic-templates
1	2	2	1	0	2	1	0	1	0	0.739918	1.0000		nonperiodic-templates
1	0	1	3	1	1	0	1	1	1	0.739918	1.0000		nonperiodic-templates
2	1	0	1	1	0	4	0	0	1	0.122325	1.0000		nonperiodic-templates
1	2	1	0	1	0	2	2	1	0	0.739918	1.0000		nonperiodic-templates
0	1	1	1	1	2	0	2	1	1	0.911413	1.0000		nonperiodic-templates
4	0	0	2	0	2	0	0	1	1	0.066882	1.0000		nonperiodic-templates
2	2	0	2	1	0	0	1	2	0	0.534146	1.0000		nonperiodic-templates

Ο	0	0	2.	1	2.	1	0	3	1	0.350485	1.0000	nonperiodic-templates
0	2.	2	2	1	1	1	1	0	0	0.739918	1.0000	nonperiodic-templates
1	0	2	1	1	1	0	0	3	1	0.733316	1.0000	nonperiodic-templates
0	1	2.	2.	0	0	1	0	3	1	0.350485	1.0000	nonperiodic-templates
-	_	_	_		-	_	-		_			
1	1	1	1	1	0	1	1	3	0	0.739918	0.9000 *	nonperiodic-templates
0	1	2	2	1	0	1	1	0	2	0.739918	1.0000	nonperiodic-templates
2	0	0	3	1	0	1	1	2	0	0.350485	0.9000 *	nonperiodic-templates
0	0	0	2	1	2	2	0	1	2	0.534146	1.0000	nonperiodic-templates
0	1	1	0	2	4	2	0	0	0	0.066882	1.0000	nonperiodic-templates
0	2	1	2	1	0	1	2	1	0	0.739918	1.0000	nonperiodic-templates
3	0	1	1	0	0	1	2	1	1	0.534146	1.0000	nonperiodic-templates
3	1	1	1	0	1	0	1	1	1	0.739918	0.9000 *	nonperiodic-templates
0	1	0	0	2	2	1	0	2	2	0.534146	1.0000	nonperiodic-templates
1	0	2	1	1	1	1	2	1	0	0.911413	1.0000	nonperiodic-templates
1	0	0	0	4	0	4	0	0	1	0.004301	1.0000	nonperiodic-templates
1	0	0	0	1	0	1	3	2	2	0.350485	1.0000	nonperiodic-templates
2	1	2	1	0	0	0	1	1	2	0.739918	0.9000 *	nonperiodic-templates
2	0	0	1	1	1	0	2	2	1	0.739918	1.0000	nonperiodic-templates
0	1	0	0	1	2	0	1	1	4	0.122325	1.0000	nonperiodic-templates
1	0	3	0	0	0	1	1	3	1	0.213309	1.0000	nonperiodic-templates
1	0	0	1	1	0	3	1	1	2	0.534146	1.0000	nonperiodic-templates
2	2	1	0	0	1	2	2	0	0	0.534146	1.0000	nonperiodic-templates
2	1	0	0	1	0	0	3	2	1	0.350485	1.0000	nonperiodic-templates
1	1	0	0	3	0	1	2	1	1	0.534146	1.0000	nonperiodic-templates
1	1	1	2	2	0	0	2	1	0	0.739918	1.0000	nonperiodic-templates
3	1	0	2	1	0	1	1	1	0	0.534146	0.9000 *	apen
2	0	1	0	3	0	0	2	0	2	0.213309	0.9000 *	serial
0	1	1	0	1	3	0	0	2	2	0.350485	1.0000	serial

(10ns system clk $\frac{1}{2}$ cycle, 100 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets r through v and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
1	0	1	0	2	0	2	2	1	1	0.739918	1.0000	frequency
0	0	1	1	2	3	1	1	0	1	0.534146	1.0000	block-frequency
2	0	0	1	2	1	0	1	1	2	0.739918	1.0000	cumulative-sums
1	0	0	0	1	1	1	2	2	2	0.739918	1.0000	cumulative-sums
2	1	0	0	1	2	2	0	2	0	0.534146	1.0000	runs
0	0	1	0	1	1	2	2	2	1	0.739918	1.0000	fft
1	0	3	0	0	0	1	1	3	1	0.213309	1.0000	nonperiodic-templates
2	0	2	0	1	2	0	3	0	0	0.213309	0.9000 *	nonperiodic-templates
0	1	1	1	1	0	1	4	1	0	0.213309	1.0000	nonperiodic-templates
0	1	4	1	1	0	0	2	1	0	0.122325	1.0000	nonperiodic-templates
0	1	0	2	1	2	1	2	0	1	0.739918	1.0000	nonperiodic-templates
0	2	2	0	2	1	1	0	1	1	0.739918	1.0000	nonperiodic-templates
0	1	1	2	0	0	2	1	2	1	0.739918	1.0000	nonperiodic-templates
3	2	1	0	1	2	0	0	1	0	0.350485	0.8000 *	nonperiodic-templates
2	0	0	0	4	2	0	0	1	1	0.066882	1.0000	nonperiodic-templates
2	0	0	1	0	3	1	0	1	2	0.350485	1.0000	nonperiodic-templates
1	1	1	2	2	0	0	1	1	1	0.911413	1.0000	nonperiodic-templates
2	0	0	1	1	1	4	0	1	0	0.122325	0.9000 *	nonperiodic-templates
0	1	1	2	4	0	0	0	1	1	0.122325	1.0000	nonperiodic-templates
0	0	0	0	2	1 2	1	3	2	1	0.350485	1.0000	nonperiodic-templates
2	0 2	1	1	0	0	1	1 2	0	0	0.350485 0.213309	0.9000 * 0.8000 *	nonperiodic-templates nonperiodic-templates
3	1	0	2	1	1	1	1	0	0	0.534146	0.8000 *	nonperiodic-templates
1	1	0	1	0	2	1	2	1	1	0.911413	0.9000 *	nonperiodic-templates
2	0	1	1	1	2	0	1	2	0	0.739918	0.9000 *	nonperiodic-templates
2	2	0	2	1	1	0	0	1	1	0.739918	1.0000	nonperiodic-templates
2	0	0	2	0	1	2	1	2	0	0.733316	1.0000	nonperiodic-templates
2	0	2	1	0	0	2	2	0	1	0.534146	1.0000	nonperiodic-templates
2	0	2	1	0	2	0	1	2	0	0.534146	0.9000 *	nonperiodic-templates
3	0	1	1	1	1	2	0	0	1	0.534146	0.9000 *	nonperiodic-templates
1	2	2	1	1	2	0	0	0	1	0.739918	1.0000	nonperiodic-templates
1	1	2	0	2	1	1	1	1	0	0.911413	1.0000	nonperiodic-templates
1	1	0	0	1	0	4	1	2	0	0.122325	1.0000	nonperiodic-templates
3	0	1	0	1	2	0	1	1	1	0.534146	1.0000	nonperiodic-templates
1	2	0	2	1	1	0	0	1	2	0.739918	1.0000	nonperiodic-templates
3	0	0	1	1	2	0	0	2	1	0.350485	0.8000 *	nonperiodic-templates
1	2	1	1	0	1	0	1	3	0	0.534146	0.9000 *	nonperiodic-templates
1	0	3	1	1	1	1	1	1	0	0.739918	0.9000 *	nonperiodic-templates
0	0	1	1	2	0	1	3	2	0	0.350485	1.0000	nonperiodic-templates
0	0	2	1	1	1	1	1	1	2	0.911413	1.0000	nonperiodic-templates
2	0	2	1	1	0	2	0	1	1	0.739918	0.9000 *	nonperiodic-templates
1	4	1	1	1	0	0	0	1	1	0.213309	0.9000 *	nonperiodic-templates
2	2	1	0	1	0	1	0	3	0	0.350485	0.9000 *	nonperiodic-templates
3	0	0	0	1	1	1	1	1	2	0.534146	0.7000 *	nonperiodic-templates
1	1	0	1	2	1	2	1	1	0	0.911413	1.0000	nonperiodic-templates
0	1	2	0	1	2	1	1	1	1	0.911413	1.0000	nonperiodic-templates
1	1	0	0	0	1	1	3	2	1	0.534146	0.9000 *	nonperiodic-templates
3	3	0	2	1	1	0	0	0	0	0.122325	1.0000	nonperiodic-templates
1	2	2	1	1	0	1	1	0	1	0.911413	1.0000	nonperiodic-templates
2	0	1	2	1	0	2	1	1	0	0.739918	1.0000	nonperiodic-templates
0	1	1	1	0	5	1	1	0	0	0.017912	1.0000	nonperiodic-templates
2	1	0	3	1	1	1	0	0	1	0.534146	1.0000	nonperiodic-templates
0	3	1	1	2	0	1	1	1	0	0.534146	1.0000	nonperiodic-templates
3	0	0	1	0	0	1	0	4	1	0.035174	1.0000	nonperiodic-templates
0	1	0	1	0	0	2	1	3	2	0.350485	1.0000	nonperiodic-templates
0	0	0	2	2	2	0	0	2	2	0.350485	1.0000	nonperiodic-templates
0	1	2	1	2	0	1	0	3	0	0.350485	1.0000	nonperiodic-templates

1	0	1	_	_	1	_	1	0	0	0 720010	1 0000		
1	0	1	2 1	0	1	0	1 2	2 2	2	0.739918	1.0000		nonperiodic-templates
0	1 1	1 2	1	0 1	1	2	0	3	0 2	0.739918 0.350485	1.0000		nonperiodic-templates nonperiodic-templates
1	2	1	0	0	0	2	0	1	3	0.350485	0.9000	*	nonperiodic-templates
0	4	0	0	0	0	2	0	3	1	0.017912	1.0000		nonperiodic-templates
1	0	2	1	1	3	1	1	0	0	0.534146	1.0000		nonperiodic-templates
0	2	1	0	0	2	1	2	1	1	0.739918	1.0000		nonperiodic-templates
3	3	0	1	0	0	2	0	1	0	0.122325	1.0000		nonperiodic-templates
1	3	3	0	0	1	0	0	1	1	0.213309	1.0000		nonperiodic-templates
0	1	1	1	0	0	1	2	2	2	0.739918	1.0000		nonperiodic-templates
0	1	2	1	3	0	1	1	0	1	0.534146	1.0000		nonperiodic-templates
0	1	0	0	0	5	1	0	1	2	0.008879	1.0000		nonperiodic-templates
2	3	0	0	0	0	1	2	0	2	0.213309	0.9000	*	nonperiodic-templates
2	0	1	0	3	0	1	1	2	0	0.350485	1.0000		nonperiodic-templates
0	0	2	0	3	0	0	2	2	1	0.213309	1.0000		nonperiodic-templates
1	3	1	1	0	1	1	1	0	1	0.739918	1.0000		nonperiodic-templates
1	1	2	0	0	2	0	1	0	3	0.350485	1.0000		nonperiodic-templates
1	2	0	0	2	2	0	0	1	2	0.534146	1.0000		nonperiodic-templates
4	1	0	0	2	3	0	0	0	0	0.017912	0.9000	*	nonperiodic-templates
1	1	0	1	0	0	0	4	3	0	0.035174	1.0000		nonperiodic-templates
0	1	0	1	0	2	2	2	2	0	0.534146	1.0000		nonperiodic-templates
0	1	1	0	0	1	1	1	4	1	0.213309	1.0000		nonperiodic-templates
1	0	1	1	1	0	1	1	2	2	0.911413	1.0000		nonperiodic-templates
1	0	1	1	0	0	1	0	4	2	0.122325	1.0000		nonperiodic-templates
1	0	1	0	1	3	1	2	1	0	0.534146	1.0000		nonperiodic-templates
3	1	2	2	0	0	1	1	0	0	0.350485	1.0000		nonperiodic-templates
0	2	0	0	2	3	2	1	0	0	0.213309	1.0000		nonperiodic-templates
3	0	0	1	1	0	1	1	2	1	0.534146	0.8000	*	nonperiodic-templates
0	0	0	1	3	0	3	1	0	2	0.122325	1.0000		nonperiodic-templates
0	1	0	1	2	1	0	1	3	1	0.534146	1.0000		nonperiodic-templates
1	0	1	2	1	0	2	1	1	1	0.911413	1.0000		nonperiodic-templates
1	2	1	0	4	1	0	1	0	0	0.122325	1.0000		nonperiodic-templates
2	1	0	0	1	2	0	2	1	1	0.739918	1.0000		nonperiodic-templates
1	2	2	0	0	1	1	1	2	0	0.739918	1.0000		nonperiodic-templates
2	1	0	1	1	1	2	1	0	1	0.911413	1.0000		nonperiodic-templates
0	2	1	0	2	2	1	0	1	1	0.739918	1.0000		nonperiodic-templates
1	1	2	0	1	3	0	1	1	0	0.534146	1.0000		nonperiodic-templates
1	0	0	1	2	1	0	2	3	0	0.350485	1.0000		nonperiodic-templates
2	1	2	0	0	0	0	0	2	3	0.213309	0.8000	*	nonperiodic-templates
0	2	0	2	1	0	2	2	0	1	0.534146	1.0000		nonperiodic-templates
0	1	1	3	0	0	1	2	1	1	0.534146	1.0000		nonperiodic-templates
0	1	0	1	1	2	0	1	3	1	0.534146	1.0000		nonperiodic-templates
2	2	0	1	1	1	1	1	1	0	0.911413	1.0000		nonperiodic-templates
1	1	0	0	1	2	1	0	1	3	0.534146	0.9000	*	nonperiodic-templates
0	1	0	2	2	2	1	2	0	0	0.534146	1.0000		nonperiodic-templates
1	2	0	2	2	0	0	2	1	0	0.534146	0.9000	*	nonperiodic-templates
2	2	0	1	1	2	0	0	1	1	0.739918	0.9000		nonperiodic-templates
2	0	0	1	2	1	1	1	2	0	0.739918	0.8000	*	nonperiodic-templates
1	0	2	1	2	0	1	1	1	1	0.911413	1.0000		nonperiodic-templates
3	2	1	1	0	0	1	2	0	0	0.350485	1.0000		nonperiodic-templates
1	1	3	1	0	1	1	0	2	0	0.534146	1.0000		nonperiodic-templates
3	0	0	0 2	2	2	0 2	0	2	1	0.213309	1.0000		nonperiodic-templates nonperiodic-templates
1	1	1	0		1	2	0 1	1 2	2 1	0.739918	1.0000		
1	1 2	1	2	0		1				0.911413	1.0000		nonperiodic-templates
0 2	0		1	2	0 1	1	1	1 2	0	0.739918	1.0000		nonperiodic-templates nonperiodic-templates
		1	1	2	1		0 1		1	0.739918			
0 1	0 1	3 1	0	1	0	0 4	1	1 0	1	0.534146 0.213309	1.0000		nonperiodic-templates nonperiodic-templates
1	0	0	0	1	2	1	3	1	1	0.534146	1.0000		nonperiodic-templates
0	1	0	0	0	0	4	0	3	2	0.017912	1.0000		nonperiodic-templates
1	0	1	2	1	0	1	1	2	1	0.017912	1.0000	*	nonperiodic-templates
0	3	1	0	1	1	0	1	2	1	0.534146	1.0000		nonperiodic-templates
0	1	2	1	0	1	1	1	2	1	0.911413	1.0000		nonperiodic-templates
0	1	2	1	0	1	1	0	3	1	0.534146	1.0000		nonperiodic-templates
2	1	2	1	0	2	2	0	0	0	0.534146	1.0000		nonperiodic-templates
1	2	2	1	0	2	1	0	1	0	0.739918	1.0000		nonperiodic-templates
1	0	1	3	1	1	0	1	1	1	0.739918	1.0000		nonperiodic-templates
2	1	0	1	1	0	4	0	0	1	0.122325	1.0000		nonperiodic-templates
1	2	1	0	1	0	2	2	1	0	0.739918	1.0000		nonperiodic-templates
0	1	1	1	1	2	0	2	1	1	0.911413	1.0000		nonperiodic-templates
4	0	0	2	0	2	0	0	1	1	0.066882	1.0000		nonperiodic-templates
													-

2.	2.	0	2.	1	0	0	1	2.	0	0.534146	1.0000		nonperiodic-templates
0	0	0	2	1	2	1	0	3	1	0.350485	1.0000		nonperiodic-templates
0	2	2	2	1	1	1	1	0	0	0.739918	1.0000		nonperiodic-templates
1	0	2.	1	1	1	0	0	3	1	0.739918	1.0000		nonperiodic-templates
0	_	2	2	0	0	1	0	3		0.350485	1.0000		± ±
1	1			-	•	_	-		1				nonperiodic-templates
Ţ	1	1	1	1	0	1	1	3	0	0.739918	0.9000	^	nonperiodic-templates
0	1	2	2	1	0	1	1	0	2	0.739918	1.0000		nonperiodic-templates
2	0	0	3	1	0	1	1	2	0	0.350485	0.9000	*	nonperiodic-templates
0	0	0	2	1	2	2	0	1	2	0.534146	1.0000		nonperiodic-templates
0	1	1	0	2	4	2	0	0	0	0.066882	1.0000		nonperiodic-templates
0	2	1	2	1	0	1	2	1	0	0.739918	1.0000		nonperiodic-templates
3	0	1	1	0	0	1	2	1	1	0.534146	1.0000		nonperiodic-templates
3	1	1	1	0	1	0	1	1	1	0.739918	0.9000	*	nonperiodic-templates
0	1	0	0	2	2	1	0	2	2	0.534146	1.0000		nonperiodic-templates
1	0	2	1	1	1	1	2	1	0	0.911413	1.0000		nonperiodic-templates
1	0	0	0	4	0	4	0	0	1	0.004301	1.0000		nonperiodic-templates
1	0	0	0	1	0	1	3	2	2	0.350485	1.0000		nonperiodic-templates
2	1	2	1	0	0	0	1	1	2	0.739918	0.9000	*	nonperiodic-templates
2	0	0	1	1	1	0	2	2	1	0.739918	1.0000		nonperiodic-templates
0	1	0	0	1	2	0	1	1	4	0.122325	1.0000		nonperiodic-templates
1	0	3	0	0	0	1	1	3	1	0.213309	1.0000		nonperiodic-templates
1	0	0	1	1	0	3	1	1	2	0.534146	1.0000		nonperiodic-templates
2	2	1	0	0	1	2	2	0	0	0.534146	1.0000		nonperiodic-templates
2.	1	0	0	1	0	0	3	2.	1	0.350485	1.0000		nonperiodic-templates
1	1	0	0	3	0	1	2	1	1	0.534146	1.0000		nonperiodic-templates
1	1	1	2	2	0	0	2	1	0	0.739918	1.0000		nonperiodic-templates
3	1	0	2	1	0	1	1	1	0	0.534146	0.9000	*	apen
2	0	1	0	3	0	0	2	0	2	0.213309	0.9000		serial
0	1	1	0	1	3	0	0	2	2	0.350485	1.0000		serial
U	1	1	U	1)	U	U	2	2	0.550465	1.0000		201101

For further guidelines construct a probability table using the MAPLE program provided in the addendum section of the documentation.

(10ns system clk $\frac{1}{2}$ cycle, 120 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets a through f and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
2	2	1	1	0	1	1	1	1	0	0.911413	0.9000 *	frequency
1	1	0	1	1	0	1	3	0	2	0.534146	1.0000	block-frequency
3	0	2	0	2	0	0	0	1	2	0.213309	1.0000	cumulative-sums
1	1	1	3	1	0	1	1	0	1	0.739918	0.9000 *	cumulative-sums
0	1	3	0	0	2	2	1	0	1	0.350485	1.0000	runs
1	0	1	1	0	2	1	1	2	1	0.911413	1.0000	fft
2	2	0	0	1	3	1	0	0	1	0.350485	1.0000	nonperiodic-templates
0	2	0	2	1	1	1	1	0	2	0.739918	1.0000	nonperiodic-templates
0	3	1	0	1	1	1	1	0	2	0.534146	1.0000	nonperiodic-templates
2	1	2	1	0	1	2	1	0	0	0.739918	1.0000	nonperiodic-templates
0	0	3	1	1	0	0	2	2	1	0.350485	1.0000	nonperiodic-templates
0	0	1	3	2	1	0	2	1	0	0.350485	1.0000	nonperiodic-templates
1	0	0	0	4	0	1	0	2	2	0.066882	1.0000	nonperiodic-templates
2	2	1	1	1	0	1	0	1	1	0.911413	1.0000	nonperiodic-templates
1 1	0	2	2	2	0 1	0	2	1	0	0.534146	1.0000	nonperiodic-templates nonperiodic-templates
0	2	1	0	0	1	0	0	4	2	0.213309 0.066882	1.0000	nonperiodic-templates
0	0	2	2	0	2	2	1	0	1	0.534146	1.0000 1.0000	nonperiodic-templates
1	0	0	0	1	0	2	4	0	2	0.066882	1.0000	nonperiodic-templates
0	2	2	1	1	0	1	0	0	3	0.350485	1.0000	nonperiodic-templates
0	0	0	1	1	2	2	1	1	2	0.739918	1.0000	nonperiodic-templates
1	2	1	1	1	1	1	0	2	0	0.733310	1.0000	nonperiodic-templates
1	0	2	1	0	2	1	1	1	1	0.911413	1.0000	nonperiodic-templates
1	2	0	2	0	0	0	4	0	1	0.066882	1.0000	nonperiodic-templates
2	0	0	1	0	1	4	0	1	1	0.122325	1.0000	nonperiodic-templates
1	0	1	1	1	0	3	2	0	1	0.534146	1.0000	nonperiodic-templates
1	0	0	1	1	2	1	0	1	3	0.534146	1.0000	nonperiodic-templates
3	1	0	0	1	1	0	1	2	1	0.534146	0.9000 *	nonperiodic-templates
1	2	0	2	1	0	2	0	0	2	0.534146	1.0000	nonperiodic-templates
2	0	0	2	1	0	1	3	0	1	0.350485	1.0000	nonperiodic-templates
2	3	2	0	0	0	0	1	1	1	0.350485	1.0000	nonperiodic-templates
0	1	1	0	1	1	2	3	1	0	0.534146	1.0000	nonperiodic-templates
0	1	0	1	2	0	2	1	2	1	0.739918	1.0000	nonperiodic-templates
0	1	1	2	1	1	1	1	1	1	0.991468	1.0000	nonperiodic-templates
0	1	1	0	1	1	5	1	0	0	0.017912	1.0000	nonperiodic-templates
0	2	1	1	2	2	0	0	0	2	0.534146	1.0000	nonperiodic-templates
0	1	0	2	0	0	2	3	0	2	0.213309	1.0000	nonperiodic-templates
2	0	0	1	2	0	3	1	0	1	0.350485	1.0000	nonperiodic-templates
1	2	1	0	1	2	0	0	1	2	0.739918	0.9000 *	nonperiodic-templates
0	1	0	2	1	2	0	0	2	2	0.534146	1.0000	nonperiodic-templates
2	2	1	0	2	0	0	1	0	2	0.534146	1.0000	nonperiodic-templates
0	0	1	2	0	1	2	2	2	0	0.534146	1.0000	nonperiodic-templates
0	0	1	0	1	1	3	0	3	1	0.213309	1.0000	nonperiodic-templates
1	3	0	1	2	0	0	1	0	2	0.350485	1.0000	nonperiodic-templates
1	2	0	0	0	3	1	2	0	1	0.350485	1.0000	nonperiodic-templates
0	1	0	2	0	2	1	1	1	2	0.739918	1.0000	nonperiodic-templates
1	0	0	0	2	1	1	0	3	2	0.350485	1.0000	nonperiodic-templates
1	0	1	1	0	1	1	2	1	2	0.911413	1.0000	nonperiodic-templates
1	1	2	1	0	1 2	1 2	0	2	1	0.911413	1.0000	nonperiodic-templates
0	0	0	1 2	1	2	3	1	1	1	0.911413	1.0000	nonperiodic-templates nonperiodic-templates
0	1	0	1	0	1	3 2	1	2	1		1.0000	nonperiodic-templates nonperiodic-templates
4	1	0	0	0	0	1	1	1	2	0.739918 0.122325	1.0000 0.9000 *	nonperiodic-templates nonperiodic-templates
1	0	1	2	1	3	0	1	0	1	0.122323	0.9000 *	nonperiodic-templates
2	1	0	0	0	1	1	1	2	2	0.739918	0.8000 *	nonperiodic-templates
2	1	0	2	1	0	2	2	0	0	0.733316	1.0000	nonperiodic-templates
0	1	1	1	1	1	3	0	1	1	0.739918	1.0000	nonperiodic-templates
0	1	1	1	3	2	1	0	0	1	0.534146	1.0000	nonperiodic-templates
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0	1	2	2	1	1	0	0	0	1	0 01000	1 0000		
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2	2	1	1	0	1	1	0	1	1	0.911413	1.0000		nonperiodic-templates
0	1	1	0	0	4	1	1	2	0	0.122325	1.0000		nonperiodic-templates
1	2	0	0	1	1	1	1	1	2	0.911413	1.0000		nonperiodic-templates
2	0	0	1	1	1	2	0	1	2	0.739918	1.0000		nonperiodic-templates
2	1	0	3	0	1	2	1	0	0	0.350485	1.0000		nonperiodic-templates
0	1	1	2	2	1	0	0	2	1	0.739918	1.0000		nonperiodic-templates
0	1	0	2	1	1	0	1	2	2	0.739918	1.0000		nonperiodic-templates
1	0	0	0	2	1	1	4	0	1	0.122325	1.0000		nonperiodic-templates
0	0	0	4	2	2	1	0	1	0	0.066882	1.0000		nonperiodic-templates
0	0	0	0	2	4	1	1	1	1	0.122325	1.0000		nonperiodic-templates
0	0	1	2	5	1	1	0	0	0	0.008879	1.0000		nonperiodic-templates
0	1	0	2	1	1	0	2	2	1	0.739918	1.0000		nonperiodic-templates
2	0	1	0	1	1	2	3	0	0	0.350485	0.8000	*	nonperiodic-templates
0	0	1	1	0	1	2	2	2	1	0.739918	1.0000		nonperiodic-templates
0	1	1	1	2	1	1	1	2	0	0.911413	1.0000		nonperiodic-templates
1	0	2	2	1	1	1	0	1	1	0.911413	1.0000		nonperiodic-templates
1	0	1	1	0	1	1	2	1	2	0.911413	1.0000		nonperiodic-templates
0	0	2	0	0	0	1	2	3	2	0.213309	1.0000		nonperiodic-templates
1	0	0	0	3	1	3	0	1	1	0.213309	1.0000		nonperiodic-templates
1	0	2	1	1	1	1	3	0	0	0.534146	1.0000		nonperiodic-templates
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2	2	0	1	2	0	0	2	0	1	0.534146	1.0000	*	nonperiodic-templates
2	1	1	1	2	2	0	0	0	1	0.739918	0.9000		nonperiodic-templates
2	0	1	0	0	0	2	2	2	1	0.534146	0.9000		nonperiodic-templates
0	3	1	1	1	1	1	1	1	0	0.739918	1.0000		nonperiodic-templates
0	1	1	0	1	1	2	3	1	0	0.534146	1.0000		nonperiodic-templates
0	2	1	1	0	2	0	1	3	0	0.350485	1.0000		nonperiodic-templates
2	0	2	0	0	2	1	0	2	1	0.534146	1.0000		nonperiodic-templates
0	1	0	0	1	4	1	1	0	2	0.122325	1.0000		nonperiodic-templates
1	2	2	0	0	1	0	1	1	2	0.739918	1.0000		nonperiodic-templates
1	0	1	2	0	3	2	0	1	0	0.350485	0.9000	*	nonperiodic-templates
1	0	0	1	2	2	0	1	2	1	0.739918	1.0000		nonperiodic-templates
1	0	0	1	0	0	2	0	4	2	0.066882	0.9000		nonperiodic-templates
2	0	0	2	4	1	0	0	0	1	0.066882	0.9000	*	nonperiodic-templates
2	0 1	0	1 1	0 1	1	2 1	1 1	1 2	2 1	0.739918 0.911413	1.0000		nonperiodic-templates
0	2	2	0	0	2	0	2	1	1	0.534146	1.0000		nonperiodic-templates nonperiodic-templates
1	2	0	0	0	4	1	1	1	0	0.122325	1.0000		nonperiodic-templates
1	1	1	0	0	0	1	4	1	1	0.213309	1.0000		nonperiodic-templates
0	1	3	0	0	0	1	2	0	3	0.122325	1.0000		nonperiodic-templates
1	1	0	1	1	2	0	1	2	1	0.911413	1.0000		nonperiodic-templates
0	0	0	1	0	3	2	2	2	0	0.213309	1.0000		nonperiodic-templates
1	0	0	0	0	0	4	1	2	2	0.066882	1.0000		nonperiodic-templates
1	0	1	2	0	2	1	3	0	0	0.350485	1.0000		nonperiodic-templates
1	0	0	0	1	1	1	1	2	3	0.534146	0.9000	*	nonperiodic-templates
0	1	1	0	1	2	2	0	2	1	0.739918	1.0000		nonperiodic-templates
1	2	1	0	1	1	1	2	1	0	0.911413	1.0000		nonperiodic-templates
2 1	1	1	0	2	0 1	2 1	1 2	1	0 2	0.739918	0.9000	^	nonperiodic-templates nonperiodic-templates
1	1	1	0	1	3	2	1	0	0	0.911413 0.534146	1.0000	*	nonperiodic-templates
2	0	1	2	1	0	1	3	0	0	0.350485	0.8000		nonperiodic-templates
0	1	0	1	1	0	1	3	2	1	0.534146	1.0000		nonperiodic-templates
0	2	0	1	0	2	1	1	2	1	0.739918	1.0000		nonperiodic-templates
0	1	0	2	3	0	0	1	3	0	0.122325	1.0000		nonperiodic-templates
2	1	0	1	1	1	3	0	1	0	0.534146	0.9000	*	nonperiodic-templates
1	1	2	1	2	1	1	0	0	1	0.911413	1.0000		nonperiodic-templates
1	2	0	0	0	1	1	3	1	1	0.534146	1.0000		nonperiodic-templates
1	1	1	1	0	3	0	1	2	0	0.534146	1.0000		nonperiodic-templates
0	0	2	0	0	3	1	3	1	0	0.122325	1.0000		nonperiodic-templates
1	2	0	0	2	2	1	0	0	2	0.534146	1.0000		nonperiodic-templates
1	1	0	3	0	0	2	0	1	2	0.350485	1.0000		nonperiodic-templates
0 1	0 2	0 1	1	0	2 1	2 1	2	2	1 2	0.534146 0.739918	1.0000	*	nonperiodic-templates nonperiodic-templates
2	0	2	0	1	1	1	1	2	0	0.739918	0.9000		nonperiodic-templates
0	2	0	1	0	1	0	3	3	0	0.122325	1.0000		nonperiodic-templates
0	2	1	1	0	1	1	2	0	2	0.739918	1.0000		nonperiodic-templates
0	1	1	2	2	0	2	1	1	0	0.739918	1.0000		nonperiodic-templates
1	2	1	1	1	0	0	1	1	2	0.911413	1.0000		nonperiodic-templates

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0 1 1 3 0 2 1 1 0 1 0.534146 1.0000 nonper	riodic-templates
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2 0 2 1 2 0 0 2 1 0 0.534146 1.0000 nonper	riodic-templates
2 1 1 0 2 0 1 1 2 0 0.739918 0.9000 * nonper	riodic-templates
0 0 0 1 2 1 0 1 3 2 0.350485 1.0000 nonper	riodic-templates
1 1 1 0 1 1 0 2 2 1 0.911413 1.0000 nonper	riodic-templates
1 0 3 1 1 1 1 2 0 0 0.534146 1.0000 nonper	riodic-templates
3 1 2 0 1 0 0 2 1 0 0.350485 0.9000 * nonper	riodic-templates
3 1 0 3 1 1 0 1 0 0 0.213309 1.0000 nonper	riodic-templates
2 2 0 1 2 1 0 1 0 1 0.739918 1.0000 nonper	riodic-templates
3 0 0 1 1 2 1 1 1 0 0.534146 1.0000 nonper	riodic-templates
	riodic-templates
1 1 0 0 0 0 1 4 2 1 0.122325 1.0000 nonper	riodic-templates
2 2 0 0 1 2 2 0 0 1 0.534146 1.0000 nonper	riodic-templates
2 0 0 2 1 0 2 0 2 1 0.534146 0.9000 * nonper	riodic-templates
1 2 1 0 2 0 2 1 1 0 0.739918 1.0000 nonper	riodic-templates
0 1 1 1 1 2 1 1 1 0.991468 1.0000 nonper	riodic-templates
1 3 0 1 0 0 3 1 1 0 0.213309 0.9000 * nonper	riodic-templates
1 0 1 2 1 1 0 0 1 3 0.534146 1.0000 nonper	riodic-templates
0 0 3 1 3 2 0 1 0 0 0.122325 1.0000 apen	-
1 0 4 1 1 0 1 1 1 0 0.213309 1.0000 seria	1
1 2 0 3 2 0 0 0 1 1 0.350485 1.0000 serial	1

(10ns system clk $\frac{1}{2}$ cycle, 120 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets 1 through q and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
0	0	1	0	2	2	1	1	1	2	0.739918	1.0000	frequency
1	0	1	1	2	1	2	0	1	1	0.911413	1.0000	block-frequency
0	0	3	1	0	0	1	3	0	2	0.122325	1.0000	cumulative-sums
0	1	2	1	0	2	1	0	2	1	0.739918	1.0000	cumulative-sums
1	2	0	0	0	0	2	1	4	0	0.066882	1.0000	runs
0	0	1	2	2	1	1	2	1	0	0.739918	1.0000	fft
2	1	1	1	0	2	1	2	0	0	0.739918	0.9000 *	nonperiodic-templates
1	0	2	1	0	2	1	2	1	0	0.739918	1.0000	nonperiodic-templates
2	0	1	1	1	0	0	2	2	1	0.739918	1.0000	nonperiodic-templates
0	0	2	1	1	1	2	2	1	0	0.739918	1.0000	nonperiodic-templates
1	2	0	1	0	1	0	2	0	3	0.350485	1.0000	nonperiodic-templates
2	2	1	0	1	3	0	0	0	1	0.350485	1.0000	nonperiodic-templates
0	1	2	1	1	0	1	1	1	2	0.911413	1.0000	nonperiodic-templates
2	1	1	2	0	2	0	1	1	0	0.739918	1.0000	nonperiodic-templates
2	0	1	1	0 2	2	1	2	0	1 2	0.739918	1.0000	nonperiodic-templates nonperiodic-templates
0	0	0	3	1	0	1	1	4	0	0.739918 0.035174	1.0000	nonperiodic-templates
0	0	1	2	0	2	2	0	0	3	0.213309	1.0000	nonperiodic-templates
1	0	2	1	1	1	0	1	1	2	0.911413	1.0000	nonperiodic-templates
1	1	1	2	3	0	0	1	0	1	0.534146	1.0000	nonperiodic-templates
0	0	1	2	0	0	1	4	1	1	0.122325	1.0000	nonperiodic-templates
1	1	0	2	1	2	1	1	0	1	0.911413	1.0000	nonperiodic-templates
1	1	0	0	0	0	1	3	2	2	0.350485	1.0000	nonperiodic-templates
0	2	1	1	1	0	1	1	1	2	0.911413	1.0000	nonperiodic-templates
0	0	1	0	2	4	2	1	0	0	0.066882	1.0000	nonperiodic-templates
0	2	1	3	1	0	2	0	1	0	0.350485	1.0000	nonperiodic-templates
0	3	0	0	0	0	1	3	1	2	0.122325	1.0000	nonperiodic-templates
1	1	0	2	0	1	3	0	1	1	0.534146	1.0000	nonperiodic-templates
1	1	1	1	1	0	1	2	2	0	0.911413	1.0000	nonperiodic-templates
0	2	0	1	1	0	3	1	0	2	0.350485	1.0000	nonperiodic-templates
2	1	0	1	1	0	1	0	3	1	0.534146	1.0000	nonperiodic-templates
1	3	0	0	1	2	0	2	1	0	0.350485	0.9000 *	nonperiodic-templates
1	0	1	1	0	1	1	4	1	0	0.213309	1.0000	nonperiodic-templates
1	1	0	1	1	1	1	1	2	1	0.991468	1.0000	nonperiodic-templates
1	2	0	0	1	2	1	0	1	2	0.739918	1.0000	nonperiodic-templates
0	0	1	0	4	1	0	2	1	1	0.122325	1.0000	nonperiodic-templates
0	3	2	0	1	0	1	2	0	1	0.350485	1.0000	nonperiodic-templates
0	0	1	0	3	1	2	0	0	3	0.122325	1.0000	nonperiodic-templates
1	0	1	0	0	2	3	2	1	0	0.350485	1.0000	nonperiodic-templates
1	1	0	1	1	2	1	0	2	1	0.911413	0.9000 *	nonperiodic-templates
3	0	0	0	1	1	1	1	1	2	0.534146	0.9000 *	nonperiodic-templates
0	1	0	1	2	1	2	1	1	1	0.911413	1.0000	nonperiodic-templates
1	1	0	1	2	2	1	1	0	1	0.911413	1.0000	nonperiodic-templates
1	1	2	0	3	0	0	0	2	1	0.350485	1.0000	nonperiodic-templates
1	1	0	3	0	0	1	0	2	2	0.350485	1.0000	nonperiodic-templates
0	0	0	1	3	1	2	0	2	1	0.350485	1.0000	nonperiodic-templates
1	0 2	0	1 4	0	3	2	0	1	2	0.350485	1.0000	nonperiodic-templates nonperiodic-templates
0	0	2	0	0	1	2	1	3	1	0.066882	1.0000	nonperiodic-templates
1	1	0	1	2	1	1	2	1	0	0.350485 0.911413	1.0000	nonperiodic-templates
1	1	1	1	2	1	1	0	1	1	0.911413	1.0000 1.0000	nonperiodic-templates
3	1	0	1	0	1	3	1	0	0	0.213309	1.0000	nonperiodic-templates
1	0	2	1	3	0	0	0	2	1	0.350485	0.9000 *	nonperiodic-templates
0	3	0	0	1	3	0	0	1	2	0.122325	1.0000	nonperiodic-templates
1	1	0	3	0	0	2	2	0	1	0.350485	1.0000	nonperiodic-templates
1	0	0	1	3	2	1	1	1	0	0.534146	0.9000 *	nonperiodic-templates
0	1	0	1	1	4	2	1	0	0	0.122325	1.0000	nonperiodic-templates
2	0	0	2	2	1	1	0	2	0	0.534146	1.0000	nonperiodic-templates
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1	1	0	0	3	2.	0	1	2.	0	0.350485	1.0000	nonperiodic-templates
2	1	2	2	0	1	1	0	0	1	0.739918	1.0000	nonperiodic-templates
2	0	0	1	3	0	2	1	1	0	0.350485	0.9000 *	
2	0	0	3	2	1	0	0	0	2.	0.213309	1.0000	nonperiodic-templates
3	2	0	1	1	0	0	0	3	0	0.122325	1.0000	nonperiodic-templates
1	3	1	0	0	1	1	1	2.	0	0.534146	0.9000 *	
1	1	1	0	1	0	2	2	2	0	0.739918	1.0000	nonperiodic-templates
2	1	1	1	0	0	2	1	0	2	0.739918	1.0000	nonperiodic-templates
1	1	0	3	1	1	0	0	2	1	0.534146	0.9000 *	
0	2	0	2	1	1	0	0	1	3	0.350485	1.0000	nonperiodic-templates
1	2	1	1	1	1	0	0	1	2	0.911413	1.0000	nonperiodic-templates
1	0	1	1	1	2	0	0	3	1	0.534146	0.9000 *	
2	0	1	1	1	0	2	3	0	0	0.350485	1.0000	nonperiodic-templates
2	1	1	2	1	0	0	2	1	0	0.739918	1.0000	nonperiodic-templates
0	0	3	0	2	1	1	0	1	2	0.350485	1.0000	nonperiodic-templates
2	2.	2	0	0	1	2	0	1	0	0.534146	0.9000 *	
2	0	1	2	1	2	1	0	1	0	0.739918	1.0000	nonperiodic-templates
0	1	3	1	0	1	0	1	2	1	0.733310	1.0000	nonperiodic-templates
1	0	0	2	3	1	1	0	1	1	0.534146	1.0000	nonperiodic-templates
2	1	1	1	0	2	1	2	0	0	0.739918	0.9000 *	± ±
0	0	0	1	2.	2	2.	2	0	1	0.733310	1.0000	nonperiodic-templates
2.	3	0	0	1	1	2	1	0	0	0.350485	1.0000	nonperiodic-templates
1	0	2	2	2.	1	1	1	0	0	0.739918	1.0000	nonperiodic-templates
0	0	0	0	0	3	0	2	1	4	0.733310	1.0000	nonperiodic-templates
1	1	3	1	1	0	1	1	1	0	0.739918	1.0000	nonperiodic-templates
0	2.	0	0	1	3	0	2	2	0	0.733310	1.0000	apen
1	0	0	1	0	1	3	2	1	1	0.534146	1.0000	serial
1	0	0	1	2	1	1	0	2.	2	0.739918	0.9000 *	
Τ.	U	U	_	_	Τ.	Τ.	U	_	_	0.100010	0.3000 ~	2⊂⊤ ⊤α ⊤

(10ns system clk $\frac{1}{2}$ cycle, 140 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets 1 through q and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.0000 *	frequency
8	2	0	0	0	0	0	0	0	0	0.000000	* 0.5000 *	block-frequency
10	0	0	0	0	0	0	0	0	0	0.000000		cumulative-sums
10	0	0	0	0	0	0	0	0	0	0.000000		cumulative-sums
7	0	0	0	1	1	0	1	0	0	0.000003		runs
0	2 1	0 3	0	0 2	3	2	0	2	1	0.213309 0.350485	1.0000 0.9000 *	fft
2 3	1	2	1	0	0	0	2	1	0	0.350485	1.0000	nonperiodic-templates nonperiodic-templates
3	0	0	1	0	0	3	0	1	2	0.122325	1.0000	nonperiodic-templates
3	1	2	0	0	1	0	1	1	1	0.534146	1.0000	nonperiodic-templates
1	2	0	1	0	0	0	3	3	0	0.122325	0.9000 *	nonperiodic-templates
1	1	1	1	3	1	2	0	0	0	0.534146	1.0000	nonperiodic-templates
0	1	1	1	0	1	1	3	0	2	0.534146	1.0000	nonperiodic-templates
1	2	0	0	1	2	2	2	0	0	0.534146	1.0000	nonperiodic-templates
3	1	1	0	1	1	0	0	2	1	0.534146	0.9000 *	nonperiodic-templates
0	2	1	0	2	1	2	1	1	0	0.739918	1.0000	nonperiodic-templates
1	1	0	2	0	1	1	2	2	0	0.739918	1.0000	nonperiodic-templates
1	1	1	2	2	1	0 1	1	1	0	0.911413	0.9000 *	nonperiodic-templates
3	0	1	1 2	0	0 1	0	0	0	1	0.213309	0.9000 * 0.9000 *	nonperiodic-templates nonperiodic-templates
1 2	0	2	1	0	1	1	2	1	0	0.739918 0.739918	1.0000	nonperiodic-templates
1	1	1	0	0	1	3	3	0	0	0.213309	1.0000	nonperiodic-templates
3	1	0	0	0	1	1	2	1	1	0.534146	1.0000	nonperiodic-templates
2	0	0	0	2	0	1	2	1	2	0.534146	0.8000 *	nonperiodic-templates
0	1	0	0	0	2	3	1	0	3	0.122325	1.0000	nonperiodic-templates
2	2	1	0	1	1	1	1	1	0	0.911413	1.0000	nonperiodic-templates
3	0	1	2	1	1	0	0	1	1	0.534146	0.9000 *	nonperiodic-templates
1	1	1	1	2	1	1	1	1	0	0.991468	0.9000 *	nonperiodic-templates
0	1	0	0	1	1	3	2	0	2	0.350485	1.0000	nonperiodic-templates
1	2	0	0	0	3	0	1	1	2	0.350485	0.9000 *	nonperiodic-templates
1	2	0	1	1	2	0	1	1	1	0.911413	0.9000 *	nonperiodic-templates
1 1	1	0	0	2	1	1	4	0	0	0.122325	1.0000	nonperiodic-templates
1	0	2	0	2	1	1	0	1	2	0.350485 0.739918	1.0000 1.0000	nonperiodic-templates nonperiodic-templates
0	0	1	2	2	1	1	0	0	3	0.350485	1.0000	nonperiodic-templates
0	1	0	2	1	0	0	4	1	1	0.122325	1.0000	nonperiodic-templates
1	0	0	1	0	2	1	3	1	1	0.534146	1.0000	nonperiodic-templates
0	3	1	1	0	2	1	0	1	1	0.534146	1.0000	nonperiodic-templates
2	1	0	1	2	1	1	0	0	2	0.739918	1.0000	nonperiodic-templates
2	1	0	1	1	1	0	1	3	0	0.534146	0.9000 *	nonperiodic-templates
1	2	1	0	1	0	1	1	3	0	0.534146	1.0000	nonperiodic-templates
2	1	0	1	2	0	1	0	2	1	0.739918	0.9000 *	nonperiodic-templates
1	2	0	0	1	2	2	0	1	1	0.739918	0.9000 *	nonperiodic-templates
0	0	0	2	1	2	1	1	3	0	0.350485	1.0000	nonperiodic-templates
1	1	0	1	0	0	3 1	1	2	1	0.534146	1.0000	nonperiodic-templates nonperiodic-templates
1 1	0 1	1	1	2	0 1	0	1 1	2	1	0.911413 0.739918	1.0000 1.0000	nonperiodic-templates
2	0	0	1	1	1	1	2	1	1	0.739918	0.9000 *	nonperiodic-templates
1	2	0	0	0	2	2	1	1	1	0.739918	1.0000	nonperiodic-templates
0	1	0	4	0	1	2	1	0	1	0.122325	1.0000	nonperiodic-templates
0	0	1	0	0	1	4	0	2	2	0.066882	1.0000	nonperiodic-templates
2	3	0	0	0	1	1	2	0	1	0.350485	0.9000 *	nonperiodic-templates
1	1	0	2	2	1	1	1	1	0	0.911413	1.0000	nonperiodic-templates
0	0	3	0	2	1	0	1	1	2	0.350485	1.0000	nonperiodic-templates
1	0	4	0	0	0	1	0	3	1	0.035174	1.0000	nonperiodic-templates
0	0	1	1	0	1	2	0	3	2	0.350485	1.0000	nonperiodic-templates
0	0	2	1	1	1	2	1	1	1	0.911413	1.0000	nonperiodic-templates
1	0	1	1	1	1	2	2	1	0	0.911413	1.0000	nonperiodic-templates

1	1	0	4	1	1	2	0	0	0	0.122325	1.0000		nonperiodic-templates
1	0	1	1	0	0	3	0	1	3	0.122323	1.0000		nonperiodic-templates
1	0	0	2	1	1	0	0	3	2	0.350485	1.0000		nonperiodic-templates
1	1	2	0	0	1	2	1	2	0	0.739918	1.0000		nonperiodic-templates
1	1	1	1	1	0	2	3	0	0	0.534146	1.0000		nonperiodic-templates
0	0	1	2	0	2	2	2	0	1	0.534146	1.0000		nonperiodic-templates
2	1	0	1	2	0	1	0	3	0	0.350485	0.9000	*	nonperiodic-templates
4	2	0	0	0	3	0	0	1	0	0.017912	1.0000		nonperiodic-templates
0	2	1	3	0	0	0	1	3	0	0.122325	1.0000		nonperiodic-templates
1	0	2	0	2	4	1	0	0	0	0.066882	1.0000		nonperiodic-templates
2	1	1	1	1	0	1	0	2	1	0.911413	1.0000		nonperiodic-templates
2	0	2	0	1	3	0	1	1	0	0.350485	0.9000	*	nonperiodic-templates
1	2	0	0	1	0	1	3	0	2	0.350485	0.9000	*	nonperiodic-templates
1	1	1	3	0	2	0	0	1	1	0.534146	1.0000		nonperiodic-templates
1	0	0	2	0	2	1	2	1	1	0.739918	1.0000		nonperiodic-templates
0	1	0	3	0	0	2	2	2	0	0.213309	1.0000		nonperiodic-templates
1	1	1	1	1	1	2	1	0	1	0.991468	1.0000		nonperiodic-templates
1	0	1	1	2	0	3	1	1	0	0.534146	1.0000		nonperiodic-templates
2	1	2	2	0	0	1	2	0	0	0.534146	0.9000	*	nonperiodic-templates
0	0	2	0	4	1	0	2	1	0	0.066882	1.0000	_	nonperiodic-templates
1	2	1	1	2	1	1	1	0	0	0.911413	0.9000	^	nonperiodic-templates
0	0 1	1 2	0	2 1	0 2	0 1	3 1	3 0	1 2	0.122325 0.739918	1.0000		nonperiodic-templates nonperiodic-templates
0	2	0	0	2	3	2	1	0	0	0.739918	1.0000		nonperiodic-templates
3	0	0	2	0	0	0	1	1	3	0.122325	0.9000	*	nonperiodic-templates
1	0	1	1	0	0	1	3	2	1	0.534146	0.9000		nonperiodic-templates
0	0	0	1	3	2	1	1	1	1	0.534146	1.0000		nonperiodic-templates
0	0	0	0	1	3	1	2	3	0	0.122325	1.0000		nonperiodic-templates
1	1	0	2	0	0	1	3	1	1	0.534146	1.0000		nonperiodic-templates
3	1	1	0	1	1	1	1	1	0	0.739918	1.0000		nonperiodic-templates
1	0	0	0	1	3	1	1	3	0	0.213309	1.0000		nonperiodic-templates
2	0	0	1	2	1	1	0	1	2	0.739918	0.9000	*	nonperiodic-templates
2	1	2	0	1	0	1	0	1	2	0.739918	1.0000		nonperiodic-templates
1	1	1	1	1	0	1	0	2	2	0.911413	1.0000		nonperiodic-templates
1	1	0	1	1	2	1	1	1	1	0.991468	1.0000		nonperiodic-templates
0 2	1 2	0 1	0	1 1	5 1	1	2	0 1	0 1	0.008879	1.0000		nonperiodic-templates
0	1	0	0 2	1	0	1 1	3	2	0	0.911413 0.350485	1.0000		nonperiodic-templates nonperiodic-templates
0	0	2	2	2	0	2	1	1	0	0.534146	1.0000		nonperiodic-templates
0	1	2	2	0	2	1	1	1	0	0.739918	1.0000		nonperiodic-templates
0	1	1	0	4	1	2	1	0	0	0.122325	1.0000		nonperiodic-templates
1	0	0	0	0	1	0	2	1	5	0.008879	1.0000		nonperiodic-templates
0	1	1	1	2	1	0	1	2	1	0.911413	1.0000		nonperiodic-templates
0	3	1	1	1	0	2	1	0	1	0.534146	1.0000		nonperiodic-templates
1	1	0	1	0	2	2	0	1	2	0.739918	1.0000		nonperiodic-templates
0	0	1	1	2	2	0	3	1	0	0.350485	1.0000		nonperiodic-templates
0	0	1	2	0	0	2	1	2	2	0.534146	1.0000		nonperiodic-templates
3 2	1 1	1	0	0 4	1 1	0	2	1	1	0.534146 0.066882	1.0000	*	nonperiodic-templates
2	0	2	0	0	1	1	3	0	1	0.350485	0.9000		nonperiodic-templates nonperiodic-templates
2	2	0	2	1	2	0	1	0	0	0.534146	1.0000		nonperiodic-templates
1	1	2	0	1	3	1	0	1	0	0.534146	1.0000		nonperiodic-templates
3	2	0	4	0	0	0	1	0	0	0.017912	0.9000	*	nonperiodic-templates
1	1	0	1	2	2	0	1	1	1	0.911413	1.0000		nonperiodic-templates
2	0	0	2	1	3	1	1	0	0	0.350485	1.0000		nonperiodic-templates
1	1	0	1	1	1	2	0	3	0	0.534146	1.0000		nonperiodic-templates
0	2	2	0	5	0	0	0	0	1	0.004301	1.0000		nonperiodic-templates
2	0	1	0	2	1	0	0	1	3	0.350485	0.9000	*	nonperiodic-templates
0	2	2	0	3	2	1	0	0	0	0.213309	1.0000		nonperiodic-templates
1	1	1	1	1	0	1	2	1	1	0.991468	1.0000		nonperiodic-templates
1	0	1	0	0	1	1	1	2	3	0.534146	1.0000		nonperiodic-templates
0	1 0	1	1 2	1 2	2 1	2	2	0 2	0	0.739918 0.534146	1.0000		nonperiodic-templates
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4	0	0	2	1	1	1	0	0	1	0.122325	1.0000		nonperiodic-templates nonperiodic-templates
2	1	2	0	1	0	1	0	3	0	0.350485	0.9000	*	nonperiodic-templates
0	0	0	3	0	1	0	1	4	1	0.035174	1.0000		nonperiodic-templates
0	1	2	1	0	2	2	1	1	0	0.739918	1.0000		nonperiodic-templates
1	1	2	1	1	0	0	1	2	1	0.911413	0.9000	*	nonperiodic-templates
3	0	0	2	1	1	1	0	0	2	0.350485	1.0000		nonperiodic-templates
0	0	1	1	2	1	1	1	2	1	0.911413	1.0000		nonperiodic-templates

1	1	0	2.	1	0	2.	0	0	3	0.350485	1.0000		nonperiodic-templates
0	1	2	2	1	0	1	1	0	2.	0.739918	1.0000		nonperiodic-templates
0	1	0	1	3	3	0	1	0	1	0.213309	1.0000		nonperiodic-templates
1	0	3	0	2	1	0	0	1	2	0.350485	1.0000		nonperiodic-templates
0	2	0	1	0	1	0	2	1	3	0.350485	1.0000		nonperiodic-templates
0	0	0	0	0	1	0	2	3	4	0.017912	1.0000		nonperiodic-templates
1	0	1	1	1	1	2	2	1	0	0.911413	1.0000		nonperiodic-templates
0	0	1	0	0	3	2	1	2	1	0.350485	1.0000		nonperiodic-templates
0	3	0	0	0	1	1	2	1	2	0.350485	1.0000		nonperiodic-templates
0	1	0	2	0	2	1	1	1	2	0.739918	1.0000		nonperiodic-templates
1	0	2	2	3	0	1	0	1	0	0.350485	1.0000		nonperiodic-templates
0	1	1	1	1	1	4	1	0	0	0.213309	1.0000		nonperiodic-templates
1	0	2	0	0	1	0	1	1	4	0.122325	1.0000		nonperiodic-templates
1	0	1	0	1	1	2	2	2	0	0.739918	1.0000		nonperiodic-templates
0	0	4	1	0	1	0	0	2	2	0.066882	1.0000		nonperiodic-templates
1	0	3	2	0	2	1	0	1	0	0.350485	1.0000		nonperiodic-templates
1	0	0	1	1	2	0	1	2	2	0.739918	1.0000		nonperiodic-templates
0	1	0	0	2	1	3	2	0	1	0.350485	1.0000		nonperiodic-templates
1	0	2	1	2	1	0	2	0	1	0.739918	1.0000		nonperiodic-templates
2	1	3	1	2	0	0	0	1	0	0.350485	0.9000	*	nonperiodic-templates
3	3	0	0	1	0	1	0	2	0	0.122325	0.9000	*	nonperiodic-templates
1	0	3	1	0	1	2	0	1	1	0.534146	0.9000	*	nonperiodic-templates
2	1	0	1	0	0	2	3	1	0	0.350485	1.0000		nonperiodic-templates
0	1	0	1	1	1	0	4	2	0	0.122325	1.0000		nonperiodic-templates
4	1	0	2	0	1	1	1	0	0	0.122325	0.9000	*	nonperiodic-templates
6	2	0	1	1	0	0	0	0	0	0.000199	1.0000		apen
1	0	1	4	1	1	1	0	0	1	0.213309	1.0000		serial
0	0	0	1	1	0	0	2	2	4	0.066882	1.0000		serial

(10ns system clk $\frac{1}{2}$ cycle, 140 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets r through v and consecutive outputs Xored)

 C1	 C2				 C6	 C7			C10	P-VALUE	 PI	 ROPORTIC		STATISTICAL TEST
10	0	0	0	0	0	0	0	0	0	0.000000	*			frequency
4	2	2	1	0	0	0	1	0	0	0.066882			*	block-frequency
10	0	0	0	0	0	0	0	0	0	0.000000				cumulative-sums
9	1	0	0	0	0	0	0	0	0	0.000000	*		*	cumulative-sums
5	0	1 2	0	0	2	0	2	0	0	0.004301		0.5000	*	runs
0	0 3	0	1	2	0	1	3 1	1	0 1	0.350485 0.213309		1.0000	4	fft
3 3	0	1	1	0	0	2	1	1	1	0.534146		0.8000		nonperiodic-templates nonperiodic-templates
3	2	0	0	1	0	1	2	1	0	0.350485		0.9000	,	nonperiodic-templates
0	1	0	1	1	1	1	3	2	0	0.534146		1.0000		nonperiodic-templates
1	2	2	0	2	0	1	1	0	1	0.739918		1.0000		nonperiodic-templates
0	1	1	2	1	2	2	0	1	0	0.739918		1.0000		nonperiodic-templates
1	1	1	0	0	2	2	2	0	1	0.739918		0.9000	*	nonperiodic-templates
1	0	1	2	2	0	1	0	1	2	0.739918		1.0000		nonperiodic-templates
3	1	0	0	0	1	3	0	2	0	0.122325		0.9000	*	nonperiodic-templates
1	2	1	2	1	0	0	3	0	0	0.350485		0.9000		nonperiodic-templates
1	0	4	0	1	0	0	0	1	3	0.035174		0.9000		nonperiodic-templates
2	1	0	0	1	2	0	2	1	1	0.739918		1.0000		nonperiodic-templates
0	1	0	2	0	1	1	2	1	2	0.739918		1.0000		nonperiodic-templates
0	0	1	0	2	2	0	1	2	2	0.534146		1.0000		nonperiodic-templates
0	2	3	1	0	1	2	0	1	0	0.350485		1.0000		nonperiodic-templates
1	0	2	1	0	1	2	0	2	1	0.739918		1.0000		nonperiodic-templates
2	2	1	0	0	1	0	2	1	1	0.739918		1.0000		nonperiodic-templates
1	1	1	2	0	2	2	0	0	1	0.739918		0.9000	*	nonperiodic-templates
4	1	0	0	2	1	0	0	1	1	0.122325		1.0000		nonperiodic-templates
1	1	1	0	0	1	3	0	2	1	0.534146		1.0000		nonperiodic-templates
1	2	1	1	0	1	2	1	0	1	0.911413		1.0000		nonperiodic-templates
2	0	0	0	1	4	1	2	0	0	0.066882		1.0000		nonperiodic-templates
0	0	0	1	1	0	3	2	2	1	0.350485		1.0000		nonperiodic-templates
3	2	0	0	0	0	2	1	1	1	0.350485		1.0000		nonperiodic-templates
0	1	0	1	1	1	1	2	1	2	0.911413		1.0000		nonperiodic-templates
1	0	0	0	2	2	1	1	0	3	0.350485		1.0000		nonperiodic-templates
2	2	0	0	0	1	3	0	1	1	0.350485		1.0000		nonperiodic-templates
0	1	0	0 3	1	2	1	1	1	3	0.534146		1.0000	_	nonperiodic-templates
2	0			2	0	0		1	1	0.350485		0.8000		nonperiodic-templates
2	2	1	1	0 2	1	0 1	0 1	2	1	0.739918		0.9000	^	nonperiodic-templates
2	1	1	0	2	2	1	0	1	0	0.534146 0.739918		1.0000		nonperiodic-templates nonperiodic-templates
1	1	0	1	0	1	1	1	3	1	0.739918		1.0000		nonperiodic-templates
2	2	1	1	0	1	1	1	0	1	0.733310		1.0000		nonperiodic-templates
3	1	2	0	1	0	0	2	1	0	0.350485		0.9000	*	nonperiodic-templates
2	2	0	0	1	0	1	2	1	1	0.739918		0.8000		nonperiodic-templates
1	0	2	1	1	0	2	1	2	0	0.739918		1.0000		nonperiodic-templates
1	2	0	0	2	0	1	3	1	0	0.350485		1.0000		nonperiodic-templates
2	0	1	1	4	0	2	0	0	0	0.066882		1.0000		nonperiodic-templates
1	0	1	2	1	1	0	1	1	2	0.911413		1.0000		nonperiodic-templates
1	2	2	0	1	2	1	0	1	0	0.739918		1.0000		nonperiodic-templates
0	4	2	0	1	0	1	0	2	0	0.066882		1.0000		nonperiodic-templates
1	0	0	2	1	1	1	1	1	2	0.911413		1.0000		nonperiodic-templates
0	1	0	1	0	1	3	1	1	2	0.534146		1.0000		nonperiodic-templates
1	0	1	0	1	1	2	1	2	1	0.911413		0.9000	*	nonperiodic-templates
1	0	0	0	3	1	0	1	1	3	0.213309		0.9000	*	nonperiodic-templates
0	1	1	0	4	0	0	2	2	0	0.066882		1.0000		nonperiodic-templates
2	2	0	1	1	0	2	1	0	1	0.739918		1.0000		nonperiodic-templates
1	1	0	2	0	0	1	1	3	1	0.534146		1.0000		nonperiodic-templates
1	1	2	2	1	0	1	0	2	0	0.739918		1.0000		nonperiodic-templates
0	0	1	1	2	0	1	1	4	0	0.122325		1.0000		nonperiodic-templates

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0	0	3	2	0	0	1	2	0	2	0.213309	1.0000		nonperiodic-templates
0	0	0	1	2	2	1	3	1	0	0.350485	1.0000		nonperiodic-templates
1	1	2	0	2	0	2	0	0	2	0.534146	1.0000		nonperiodic-templates
0	0	0	2	2	1	0	2	2	1	0.534146	1.0000		nonperiodic-templates
0	2	0	2	0	0	1	0	5	0	0.004301	1.0000		nonperiodic-templates
0	0	2	0	2	0	0	4	1	1	0.066882	1.0000		nonperiodic-templates
0	0	2	0	1	2	1	3	1	0	0.350485	1.0000		nonperiodic-templates
0	2	0	1	0	1	1	0	3	2	0.350485	1.0000		nonperiodic-templates
0	1	2	0	2	0	4	1	0	0	0.066882	1.0000		nonperiodic-templates
0	3	0	1	0	0	1	3	2	0	0.122325	1.0000		nonperiodic-templates
0	0	0	0	1	2	2	3	1	1	0.350485	1.0000		nonperiodic-templates
2	2	1	0	1	0	1	1	0	2	0.739918	1.0000		nonperiodic-templates
2	1	2	0	1	0	1	2	0	1	0.739918	0.9000	*	nonperiodic-templates
2	0	1	2	1	1	1	0	1	1	0.911413	0.9000	*	nonperiodic-templates
0	0	1	4	0	0	0	1	3	1	0.035174	1.0000		nonperiodic-templates
2	0	1	1	0	0	2	2	0	2	0.534146	0.9000	*	nonperiodic-templates
0	0	0	0	0	2	5	0	2	1	0.004301	1.0000		nonperiodic-templates
0	0	0	0	1	1	3	1	1	3	0.213309	1.0000		nonperiodic-templates
1	0	0	0	3	0	2	2	1	1	0.350485	1.0000		nonperiodic-templates
0	1	1	0	0	1	1	1	3	2	0.534146	1.0000		nonperiodic-templates
3	3	0	1	0	0	1	1	0	1	0.213309	0.8000	*	nonperiodic-templates
3	1	1	1	0	1	0	1	0	2	0.534146	0.8000	*	nonperiodic-templates
1	1	0	1	0	1	0	2	2	2	0.739918	0.9000	*	nonperiodic-templates
2	1	1	2	0	0	1	1	1	1	0.911413	0.8000	*	nonperiodic-templates
2	1	1	3	0	2	0	1	0	0	0.350485	0.9000	*	nonperiodic-templates
0	1	2	1	0	2	0	1	1	2	0.739918	1.0000		nonperiodic-templates
5	1	1	1	0	1	0	0	1	0	0.017912	0.9000	*	apen
3	2	1	2	0	0	1	0	0	1	0.350485	1.0000		serial
1	2	1	0	1	1	0	2	1	1	0.911413	1.0000		serial

The minimum pass rate for each statistical test with the exception of the random

The minimum pass rate for each statistical test with the exception of the random excursion (variant) test is approximately = 0.895607 for a sample size = 10 binary sequences.

For further guidelines construct a probability table using the MAPLE program provided in the addendum section of the documentation.

(10ns system clk $\frac{1}{2}$ cycle, 160 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets 1 through q and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	С6	C7	C8	С9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
7	0	1	0	1	0	0	0	1	0	0.000003	* 0.9000 *	frequency
1	2	2	1	1	0	1	1	0	1	0.911413	1.0000	block-frequency
7	1	0	0	0	1	0	1	0	0	0.000003	* 0.9000 *	cumulative-sums
6	1	0	0	2	0	0	0	0	1	0.000199	0.9000 *	cumulative-sums
1	1	0	1	2	1	1	1	1	1	0.991468	1.0000	runs
1	0	1	2	1	1	2	0	1	1	0.911413	1.0000	fft
1	1	0	1	1	1	1	1	2	1	0.991468	0.9000 *	nonperiodic-templates
0	0	1	1	2	2	2	0	2	0	0.534146	1.0000	nonperiodic-templates
0	0	2	0	1	1	2	2	1	1	0.739918	1.0000	nonperiodic-templates
0	0	0	0	1	0	4 2	0	2	3	0.017912	1.0000	nonperiodic-templates
0	2	1	0 2	1	1	0	1 2	1	1 2	0.739918 0.739918	1.0000	nonperiodic-templates nonperiodic-templates
3	2	1	1	2	1	0	0	0	0	0.739910	1.0000	nonperiodic-templates
1	0	2	1	0	0	2	1	1	2	0.739918	1.0000	nonperiodic-templates
0	0	2	0	2	1	1	1	3	0	0.350485	1.0000	nonperiodic-templates
0	0	0	2	0	0	2	1	2	3	0.213309	1.0000	nonperiodic-templates
0	0	3	0	2	1	0	0	3	1	0.122325	1.0000	nonperiodic-templates
1	0	1	1	0	1	0	2	3	1	0.534146	1.0000	nonperiodic-templates
1	0	0	0	1	1	2	1	2	2	0.739918	1.0000	nonperiodic-templates
1	1	1	3	1	3	0	0	0	0	0.213309	0.9000 *	nonperiodic-templates
2	0	1	0	1	2	0	1	2	1	0.739918	1.0000	nonperiodic-templates
1	1	1	2	0	1	1	1	1	1	0.991468	1.0000	nonperiodic-templates
0	0	3	1	1	1	1	1	1	1	0.739918	1.0000	nonperiodic-templates
1	1	0	1	0	0	3	1	3	0	0.213309	1.0000	nonperiodic-templates
0	1	1	0	0	1	2	2	1	2	0.739918	1.0000	nonperiodic-templates
1	0	3	2	0	0	0	1	2	1	0.350485	1.0000	nonperiodic-templates
0	0	1	1	2	0	2	1	2	1	0.739918	1.0000	nonperiodic-templates
2	0	0	2	1	3	0	1	0	1	0.350485	1.0000	nonperiodic-templates
1	0	2	1	2	2	2	0	0	0 2	0.534146	1.0000	nonperiodic-templates
1	0	0	0	1	0	0	1	0	1	0.534146	1.0000	nonperiodic-templates
1 1	0	2	2	1	0	1	1	2	0	0.122325	1.0000	nonperiodic-templates nonperiodic-templates
2	1	0	1	0	1	0	2	1	2	0.739918	0.9000 *	nonperiodic-templates
0	1	1	2	1	3	0	1	0	1	0.534146	1.0000	nonperiodic-templates
0	0	1	1	1	4	0	1	1	1	0.213309	1.0000	nonperiodic-templates
3	2	1	0	0	0	3	0	0	1	0.122325	0.9000 *	nonperiodic-templates
2	0	0	1	3	0	0	2	1	1	0.350485	1.0000	nonperiodic-templates
1	0	1	0	1	2	0	4	1	0	0.122325	1.0000	nonperiodic-templates
0	0	0	1	1	3	2	0	1	2	0.350485	1.0000	nonperiodic-templates
0	1	1	0	0	1	2	1	2	2	0.739918	1.0000	nonperiodic-templates
0	0	0	0	3	3	1	1	1	1	0.213309	1.0000	nonperiodic-templates
1	1	1	2	0	3	0	0	2	0	0.350485	0.9000 *	nonperiodic-templates
1	1	0	2	1	0	0	0	5	0	0.008879	1.0000	nonperiodic-templates
0	1	0	0	2	0	0	4	3	0	0.017912	1.0000	nonperiodic-templates
0	0	0	0	4	2	1	0	0	3	0.017912	1.0000	nonperiodic-templates
1	1	0	0	1	1	2	0	3	1	0.534146	1.0000	nonperiodic-templates
3	0	0	0	2	0	1	0	3	1	0.122325	1.0000	nonperiodic-templates
0	2	0	1	0	2	0	1	1	3	0.350485	1.0000	nonperiodic-templates
1	0	0	1	1	0	2	3	1	1	0.534146	1.0000	nonperiodic-templates
2	1	1	0	0	3	1	1	0	1	0.534146	1.0000	nonperiodic-templates
3 2	1 2	2	0	1	0	1	2	0	0	0.350485	0.9000 *	nonperiodic-templates
2	1	1 2	1	0 1	0	0 1	3 1	0	1	0.350485 0.911413	1.0000	nonperiodic-templates nonperiodic-templates
0	0	0	1	4	0	2	1	1	1	0.122325	1.0000	nonperiodic-templates nonperiodic-templates
1	1	1	2	0	2	1	0	1	1	0.122323	1.0000	nonperiodic-templates
2	2	1	3	0	0	0	0	2	0	0.213309	1.0000	nonperiodic-templates
1	2	1	0	2	1	1	0	1	1	0.911413	1.0000	nonperiodic-templates
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                                                                     nonperiodic-templates
0
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    Ω
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                                             0.213309
                                                         1.0000
                                                                     nonperiodic-templates
                       1
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                       2
                           1
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                                     0
                                         3
                                             0.534146
                                                         1.0000
                                                                     nonperiodic-templates
                                                         1.0000
         2
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                                             0.534146
1
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                                0
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                                                                     nonperiodic-templates
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             1
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                       1
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                                         2
                                             0.534146
                                                         1.0000
                                                                     nonperiodic-templates
                                                         1.0000
                  0
                                             0.350485
                                                                     nonperiodic-templates
1
    1
         0
             2
                       0
                           0
                                2
                                     3
                                         1
    0
                                     2
                                             0.122325
                                                          1.0000
                                                                     nonperiodic-templates
0
         0
             0
                  1
                       1
                           1
                                4
                                         1
    0
         2
                  1
                       2.
                           0
                                     0
                                         2.
                                             0.739918
                                                         1.0000
                                                                     nonperiodic-templates
1
             1
                                1
    0
             2
                           0
                                0
                                         1
                                             0.350485
                                                         1.0000
                                                                     nonperiodic-templates
    0
         0
                  3
                           0
                                     3
                                         0
                                             0.213309
                                                         1.0000
                                                                     nonperiodic-templates
1
             1
                       1
                                1
                                     2
0
    Ω
         2
             0
                  Ω
                       1
                           2
                                1
                                         2
                                             0.534146
                                                         1.0000
                                                                     nonperiodic-templates
                                                         0.9000 *
                                             0.122325
                                                                     nonperiodic-templates
```

0	0	1	2.	0	1	3	0	2.	1	0.350485	1.0000		nonperiodic-templates
1	1	1	0	1	1	2	0	1	2	0.911413	1.0000		nonperiodic-templates
1	0	1	1	0	0	1	3	1	2	0.534146	1.0000		nonperiodic-templates
0	1	0	1	1	1	2	0	3	1	0.534146	1.0000		nonperiodic-templates
0	3	0	0	1	2	0	1	0	3	0.122325	1.0000		nonperiodic-templates
1	0	3	0	1	1	1	1	1	1	0.739918	1.0000		nonperiodic-templates
0	1	1	0	3	0	2	0	1	2	0.350485	1.0000		nonperiodic-templates
0	1	0	1	2	3	3	0	0	0	0.122325	1.0000		nonperiodic-templates
3	0	1	0	0	1	1	2	1	1	0.534146	0.9000	*	nonperiodic-templates
0	0	0	0	1	2	2	0	3	2	0.213309	1.0000		nonperiodic-templates
0	1	0	0	0	0	3	1	3	2	0.122325	1.0000		nonperiodic-templates
2	0	1	2	1	0	0	0	3	1	0.350485	0.9000	*	nonperiodic-templates
1	1	1	2	2	0	0	1	1	1	0.911413	0.9000	*	nonperiodic-templates
2	1	0	2	0	2	0	0	2	1	0.534146	1.0000		nonperiodic-templates
1	0	2	0	2	2	2	0	1	0	0.534146	1.0000		nonperiodic-templates
0	2	2	3	0	0	0	1	0	2	0.213309	1.0000		nonperiodic-templates
1	2	1	1	1	2	0	0	2	0	0.739918	1.0000		nonperiodic-templates
1	1	2	1	1	2	0	0	1	1	0.911413	1.0000		nonperiodic-templates
2	2	0	0	0	0	0	2	3	1	0.213309	1.0000		nonperiodic-templates
2	1	2	2	0	0	2	1	0	0	0.534146	1.0000		nonperiodic-templates
1	1	0	1	1	1	1	1	2	1	0.991468	0.9000	*	nonperiodic-templates
1	0	1	0	1	1	2	2	1	1	0.911413	1.0000		nonperiodic-templates
0	0	0	0	1	0	4	1	0	4	0.004301	1.0000		nonperiodic-templates
1	0	1	0	1	3	1	0	1	2	0.534146	1.0000		nonperiodic-templates
1	0	2	1	1	0	1	3	1	0	0.534146	1.0000		nonperiodic-templates
1	0	1	1	1	2	1	1	1	1	0.991468	1.0000		nonperiodic-templates
0	1	1	0	5	0	1	1	1	0	0.017912	1.0000		apen
0	1	0	0	0	1	3	1	4	0	0.035174	1.0000		serial
1	0	0	0	1	0	2	2	1	3	0.350485	1.0000		serial

For further guidelines construct a probability table using the MAPLE program provided in the addendum section of the documentation.

160psf_24jrout_rvX

(10ns system clk $\frac{1}{2}$ cycle, 160 ps difference in frequency, 24 ps jitter zone sampled on the rising edge for data sets r through v and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
4	2	0	2	1	0	0	1	0	0	0.066882	0.8000 *	frequency
4	1	1	0	2	0	1	1	0	0	0.122325	1.0000	block-frequency
5	2	0	1	1	0	0	0	0	1	0.008879	0.8000 *	cumulative-sums
5	1	0	0	1	1	0	2	0	0	0.008879	0.8000 *	cumulative-sums
2	1	2	0	0	2	0	1	0	2	0.534146	1.0000	runs
1	1	1	1	0	0	2	1	2	1	0.911413	1.0000	fft
0	1	0	0	1	1	0	4	2	1	0.122325	1.0000	nonperiodic-templates
0	0	1	0	2	3	0	0	2	2	0.213309	1.0000	nonperiodic-templates
2	1 2	0 1	0	0 1	0 2	1	2	3	1	0.350485 0.350485	1.0000	nonperiodic-templates nonperiodic-templates
1	0	0	1	3	1	0	2	1	1	0.534146	1.0000 1.0000	nonperiodic-templates
0	0	0	1	1	1	1	2	0	4	0.122325	1.0000	nonperiodic-templates
0	1	0	1	1	2	0	1	2	2	0.739918	1.0000	nonperiodic-templates
1	0	1	0	1	2	1	0	3	1	0.534146	1.0000	nonperiodic-templates
0	0	1	3	1	1	0	2	1	1	0.534146	1.0000	nonperiodic-templates
0	1	1	1	1	2	1	1	2	0	0.911413	1.0000	nonperiodic-templates
1	1	0	0	1	2	1	2	2	0	0.739918	1.0000	nonperiodic-templates
1	0	2	1	0	2	0	1	2	1	0.739918	1.0000	nonperiodic-templates
2	0	0	1	0	1	0	1	5	0	0.008879	0.8000 *	nonperiodic-templates
2	0	1	1	0	2	0	1	3	0	0.350485	0.9000 *	nonperiodic-templates
0	3	0	1	2	1	0	0	3	0	0.122325	1.0000	nonperiodic-templates
2	0	1	0	0	3	0	2	2	0	0.213309	1.0000	nonperiodic-templates
0	0	2	0	0	2	0	2	4	0	0.035174	1.0000	nonperiodic-templates
1	1	0	0	0	3	0	2	1	2	0.350485	1.0000	nonperiodic-templates
1	0	2	0	1	2	0	2	1	1	0.739918	0.9000 *	nonperiodic-templates
1	0 1	1	0	1	3 1	0	1 2	2	1	0.534146 0.739918	1.0000 1.0000	nonperiodic-templates nonperiodic-templates
0	0	1	0	1	3	1	3	0	1	0.739910	1.0000	nonperiodic-templates
0	0	0	1	0	2	1	2	0	4	0.066882	1.0000	nonperiodic-templates
1	0	3	0	1	1	0	1	2	1	0.534146	1.0000	nonperiodic-templates
3	2	1	0	0	1	0	1	1	1	0.534146	0.8000 *	nonperiodic-templates
1	2	1	0	2	0	0	0	4	0	0.066882	1.0000	nonperiodic-templates
3	0	1	0	1	1	0	0	2	2	0.350485	1.0000	nonperiodic-templates
0	1	1	1	2	3	0	0	2	0	0.350485	1.0000	nonperiodic-templates
2	1	0	1	0	1	1	2	2	0	0.739918	0.9000 *	nonperiodic-templates
1	1	1	0	0	3	0	2	1	1	0.534146	1.0000	nonperiodic-templates
0	0	0	1	3	2	2	1	1	0	0.350485	1.0000	nonperiodic-templates
0	0	0	3	0	1	1	2	1	2	0.350485	1.0000	nonperiodic-templates
0	2	1	2	0	1	1	0	2	1	0.739918	1.0000	nonperiodic-templates
0	0	2	2	1	2	1	0	2	0	0.534146	1.0000	nonperiodic-templates
1	1	1	0	1 2	2	1	1	1	0	0.911413 0.534146	1.0000 1.0000	nonperiodic-templates nonperiodic-templates
1	2	1	1	0	2	0	1	2	0	0.739918	1.0000	nonperiodic-templates
1	3	1	0	0	2	1	1	1	0	0.733316	1.0000	nonperiodic-templates
0	1	2	0	1	0	0	3	1	2	0.350485	1.0000	nonperiodic-templates
1	2	1	0	1	1	2	0	1	1	0.911413	1.0000	nonperiodic-templates
1	1	0	2	1	2	0	0	2	1	0.739918	0.9000 *	nonperiodic-templates
2	0	1	1	0	1	1	2	2	0	0.739918	1.0000	nonperiodic-templates
1	0	2	1	0	2	0	1	1	2	0.739918	1.0000	nonperiodic-templates
1	1	1	0	0	1	1	1	3	1	0.739918	1.0000	nonperiodic-templates
3	0	0	0	2	0	0	1	1	3	0.122325	0.9000 *	nonperiodic-templates
1	0	1	2	1	2	0	1	1	1	0.911413	1.0000	nonperiodic-templates
3	1	0	1	0	2	1	1	1	0	0.534146	1.0000	nonperiodic-templates
1	0	0	4	0	2	0	3	0	0	0.017912	1.0000	nonperiodic-templates
0	0	1	1	0	2	1	0	3	2	0.350485	1.0000	nonperiodic-templates
1	2	0	2	0	2	0	1	1	1	0.739918	0.9000 *	nonperiodic-templates
0	2	0 2	0	1	3 2	1	0 3	2	1	0.350485	1.0000	nonperiodic-templates nonperiodic-templates
U	U	2	U	Τ	_	U	3	Τ	Τ	0.350485	1.0000	nonperrourc-temprates

1	0	3	2	1	0	0	2	1	0	0.350485	1.0000	nonperiodic-templates
1	2	0	1	0	3	1	1	0	1	0.534146	1.0000	nonperiodic-templates
1	0	1	1	1	2	1	1	2	0	0.911413	1.0000	nonperiodic-templates
2	0	1	0	1	2	0	0	2 1	2	0.534146	1.0000	nonperiodic-templates
1 2	3 1	2	0 1	0 1	1	1 2	1 2	1	0	0.534146 0.739918	1.0000	nonperiodic-templates nonperiodic-templates
1	0	1	1	2	0	1	1	1	2	0.739918	0.9000 *	nonperiodic-templates
1	0	0	0	1	3	3	2	0	0	0.122325	1.0000	nonperiodic-templates
1	1	2	0	0	2	1	0	2	1	0.739918	1.0000	nonperiodic-templates
2	1	2	0	0	0	1	1	2	1	0.739918	1.0000	nonperiodic-templates
1	0	2	2	1	1	1	2	0	0	0.739918	1.0000	nonperiodic-templates
1	1	2	0	1	0	2	1	1	1	0.911413	1.0000	nonperiodic-templates
0	0	1	1	0	2	1	3	0	2	0.350485	1.0000	nonperiodic-templates
1	1	1	0	0	1	0	3	2	1	0.534146	1.0000	nonperiodic-templates
1	1	0	1	0	4	0	0	1	2	0.122325	1.0000	nonperiodic-templates
2	1	1	1	1	1	0	2	1	0	0.911413	1.0000	nonperiodic-templates
2	0	1	2	0	1	0	2	2	0	0.534146	1.0000	nonperiodic-templates
0	2	0	0	3	1	0	2	1	1	0.350485	1.0000	nonperiodic-templates
0	0	2	0	1	4	1	1	1	0	0.122325	1.0000	nonperiodic-templates
1	1	1	1	0	1	2	1	2	0	0.911413	1.0000	nonperiodic-templates
2	1	2	0	0	2	0	1	2	0	0.534146	1.0000	nonperiodic-templates
1	2	0	0	0	2	0	1	3	1	0.350485	0.9000 *	nonperiodic-templates
2 1	0	1 1	2	0	2	1 1	1 2	1 2	0	0.739918 0.911413	1.0000	nonperiodic-templates
1	0	1	1 2	1 2	1 2	1	0	0	0	0.739918	1.0000	nonperiodic-templates nonperiodic-templates
1	0	0	0	2	2	0	0	3	2	0.739918	0.9000 *	nonperiodic-templates
0	0	0	0	0	2	1	3	1	3	0.122325	1.0000	nonperiodic-templates
1	1	2	2	0	2	1	0	0	1	0.739918	1.0000	nonperiodic-templates
2	0	1	2	0	0	1	1	1	2	0.739918	0.9000 *	nonperiodic-templates
0	0	1	1	3	0	1	2	1	1	0.534146	1.0000	nonperiodic-templates
2	0	1	2	0	2	0	2	0	1	0.534146	0.9000 *	nonperiodic-templates
2	0	1	1	2	2	0	0	2	0	0.534146	1.0000	nonperiodic-templates
0	0	1	0	0	3	2	3	1	0	0.122325	1.0000	nonperiodic-templates
2	1	1	0	0	1	1	0	1	3	0.534146	1.0000	nonperiodic-templates
0	2	1	0	1	1	2	1	2	0	0.739918	1.0000	nonperiodic-templates
1 1	0	1 0	1	2 1	2 3	0	0 1	2	1	0.739918 0.213309	1.0000 0.9000 *	nonperiodic-templates nonperiodic-templates
2	1	2	3	0	0	0	2	0	0	0.213309	0.9000 *	nonperiodic-templates
2	0	3	1	0	0	1	2	1	0	0.350485	1.0000	nonperiodic-templates
0	0	2	0	1	1	1	2	2	1	0.739918	1.0000	nonperiodic-templates
0	0	0	2	1	1	1	1	3	1	0.534146	1.0000	nonperiodic-templates
0	4	1	0	0	2	2	0	1	0	0.066882	1.0000	nonperiodic-templates
2	0	2	0	0	3	0	0	2	1	0.213309	1.0000	nonperiodic-templates
1	1	2	1	0	3	1	1	0	0	0.534146	1.0000	nonperiodic-templates
1	1	0	1	1	1	2	2	0	1	0.911413	1.0000	nonperiodic-templates
2	1	0	0	0	1	1	0	4	1	0.122325	1.0000	nonperiodic-templates
0 5	1	2	0	0	1	1 3	1	2	2	0.739918	1.0000	nonperiodic-templates
0	1	1 2	0 1	0 1	0 1	1	1 2	0	0 1	0.002043 0.911413	0.8000 * 1.0000	nonperiodic-templates nonperiodic-templates
3	1	1	0	0	2	1	0	1	1	0.534146	1.0000	nonperiodic-templates
3	0	0	1	0	1	0	2	2	1	0.350485	1.0000	nonperiodic-templates
1	1	1	0	1	3	1	0	2	0	0.534146	1.0000	nonperiodic-templates
1	1	1	2	0	2	0	2	0	1	0.739918	1.0000	nonperiodic-templates
1	1	3	0	1	1	1	2	0	0	0.534146	1.0000	nonperiodic-templates
2	1	0	0	0	1	1	2	3	0	0.350485	0.9000 *	nonperiodic-templates
0	0	0	1	0	6	1	1	1	0	0.000439	1.0000	nonperiodic-templates
1	0	0	1	0	2	1	0	4	1	0.122325	1.0000	nonperiodic-templates
0	2	1	1	0	1	0	2	2	1	0.739918	1.0000	nonperiodic-templates
0	1	2	0	0	4	0	0	2	1	0.066882	1.0000	nonperiodic-templates
0	0	0	2	1	1	0	2	3	1	0.350485	1.0000	nonperiodic-templates
0	0	0	1	1	2	0	1	3	2	0.350485	1.0000	nonperiodic-templates
1 2	0 1	1 0	2	1 0	1 1	1	1 2	1 1	1 2	0.991468 0.739918	0.9000 * 0.8000 *	nonperiodic-templates nonperiodic-templates
3	0	0	1	1	3	1	1	0	0	0.739918	0.9000 *	nonperiodic-templates
0	1	0	0	2	1	0	3	2	1	0.350485	1.0000	nonperiodic-templates
1	0	0	0	2	1	0	3	3	0	0.122325	0.9000 *	nonperiodic-templates
1	0	0	0	1	2	0	2	3	1	0.350485	0.9000 *	nonperiodic-templates
3	1	0	2	0	0	1	1	1	1	0.534146	0.9000 *	nonperiodic-templates
2	1	1	2	0	0	0	1	2	1	0.739918	1.0000	nonperiodic-templates
1	2	2	0	1	0	0	0	1	3	0.350485	1.0000	nonperiodic-templates
1	1	0	1	1	1	2	1	1	1	0.991468	1.0000	nonperiodic-templates

4	1	1	0	0	1	0	2	0	1	0.122325	0.9000	*	nonperiodic-templates
2	0	3	0	0	0	0	1	4	0	0.017912	0.9000	*	nonperiodic-templates
1	3	0	0	0	1	2	1	2	0	0.350485	1.0000		nonperiodic-templates
2	0	2	1	0	1	1	1	1	1	0.911413	0.8000	*	nonperiodic-templates
2	0	0	2	0	1	1	0	2	2	0.534146	1.0000		nonperiodic-templates
0	0	1	2	0	3	0	1	1	2	0.350485	1.0000		nonperiodic-templates
1	1	1	1	0	0	1	0	4	1	0.213309	1.0000		nonperiodic-templates
4	0	1	1	0	1	1	1	0	1	0.213309	1.0000		nonperiodic-templates
1	1	0	0	0	2	1	1	3	1	0.534146	1.0000		nonperiodic-templates
2	0	2	1	1	1	0	1	2	0	0.739918	1.0000		nonperiodic-templates
3	1	1	1	0	2	1	0	0	1	0.534146	1.0000		nonperiodic-templates
0	1	1	0	1	1	1	2	2	1	0.911413	1.0000		nonperiodic-templates
1	0	1	0	2	2	1	1	1	1	0.911413	1.0000		nonperiodic-templates
1	2	0	0	0	2	3	1	1	0	0.350485	1.0000		nonperiodic-templates
1	1	2	0	0	1	1	1	3	0	0.534146	1.0000		nonperiodic-templates
2	2	0	1	1	1	0	1	1	1	0.911413	0.8000	*	nonperiodic-templates
0	1	3	0	0	2	3	0	0	1	0.122325	1.0000		nonperiodic-templates
1	4	0	1	0	3	1	0	0	0	0.035174	1.0000		nonperiodic-templates
4	0	2	0	0	1	0	2	1	0	0.066882	1.0000		nonperiodic-templates
0	1	0	0	1	1	0	4	2	1	0.122325	1.0000		nonperiodic-templates
0	0	0	1	1	3	1	3	1	0	0.213309	1.0000		nonperiodic-templates
0	0	1	0	0	3	0	5	0	1	0.002043	1.0000		nonperiodic-templates
0	1	1	2	0	1	1	0	2	2	0.739918	1.0000		nonperiodic-templates
0	1	0	0	0	1	1	2	3	2	0.350485	1.0000		nonperiodic-templates
2	1	0	1	3	0	0	1	2	0	0.350485	0.9000	*	nonperiodic-templates
1	0	0	1	2	1	1	3	1	0	0.534146	1.0000		apen
0	0	3	1	0	2	1	3	0	0	0.122325	1.0000		serial
0	2	2	1	3	0	0	2	0	0	0.213309	1.0000		serial

10nsc_50psf_24jrfout_afX

(10ns system clk % cycle, 50 ps difference in frequency, 24 ps jitter zone sampled on the rising edge and falling edge for data sets a through f and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
0	1	0	2	2	2	0	1	1	1	0.739918	1.0000	frequency
3	1	1	1	1	0	0	1	0	2	0.534146	1.0000	block-frequency
0	0	2	1	0	1	2	1	2	1	0.739918	1.0000	cumulative-sums
0	1	1	0	0	1	1	3	1	2	0.534146	1.0000	cumulative-sums
2	0	2	1	2	1	0	2	0	0	0.534146	1.0000	runs
2	0	2	2	0	1	0	0	3	0	0.213309	0.9000 *	fft
1	2	1	1	2	0	0	2	1	0	0.739918	1.0000	nonperiodic-templates
1	0	2	2	0	2	0	3	0	0	0.213309	1.0000	nonperiodic-templates
0	3	1	0	0	1	0	2	2	1	0.350485	1.0000	nonperiodic-templates
1	0	2	0	1	1	1	2	0	2	0.739918	1.0000	nonperiodic-templates
1	0	0	1	1	2	0	1	4	0	0.122325	1.0000	nonperiodic-templates
2	0	1	0	1	0	1	1	3	1	0.534146	1.0000	nonperiodic-templates
0	1	1	0	0	2	0	2	3	1	0.350485	1.0000	nonperiodic-templates
1	1	0	1	0	3	0	0	3	1	0.213309	1.0000	nonperiodic-templates
1	0	1	1	0	2	0	1	2	2	0.739918	1.0000	nonperiodic-templates
1	1	0	0 1	1	3	0	2	1 2	0	0.534146	1.0000	nonperiodic-templates
1	1	2	1	0	1	0 2	1	2	1	0.739918	1.0000	nonperiodic-templates nonperiodic-templates
1 2	0	0	2	0	3	0	0	2	1	0.739918 0.213309	0.8000 *	nonperiodic-templates
1	1	1	0	2	2	0	1	2	0	0.739918		nonperiodic-templates
1	0	1	1	0	2	1	2	2	0	0.739918	1.0000	nonperiodic-templates
1	1	0	1	1	3	0	1	1	1	0.739918	1.0000	nonperiodic-templates
1	0	0	1	2	1	1	2	1	1	0.733310	0.9000 *	nonperiodic-templates
0	1	1	0	3	2	3	0	0	0	0.122325	1.0000	nonperiodic-templates
1	0	2	0	0	1	1	4	1	0	0.122325	1.0000	nonperiodic-templates
1	1	0	0	0	5	0	2	1	0	0.008879	1.0000	nonperiodic-templates
2	0	0	0	0	0	2	3	2	1	0.213309	1.0000	nonperiodic-templates
1	3	0	1	0	2	1	0	2	0	0.350485	1.0000	nonperiodic-templates
0	1	1	0	1	1	2	2	0	2	0.739918	1.0000	nonperiodic-templates
0	2	0	1	0	1	1	1	2	2	0.739918	1.0000	nonperiodic-templates
2	1	0	1	1	2	0	1	2	0	0.739918	0.9000 *	nonperiodic-templates
2	0	3	0	0	0	1	2	0	2	0.213309	0.9000 *	nonperiodic-templates
1	1	0	2	1	2	0	2	0	1	0.739918	0.9000 *	nonperiodic-templates
0	3	0	0	2	3	1	0	0	1	0.122325	1.0000	nonperiodic-templates
0	0	2	0	1	1	1	2	1	2	0.739918	1.0000	nonperiodic-templates
0	2	3	0	1	1	0	1	1	1	0.534146	1.0000	nonperiodic-templates
2	3	2	0	0	1	0	2	0	0	0.213309	1.0000	nonperiodic-templates
0	0	0	2	1	2	0	1	2	2	0.534146	1.0000	nonperiodic-templates
0	0	2	2	1	2	0	0	2	1	0.534146	1.0000	nonperiodic-templates
0	0	2	2	2	1	0	3	0	0	0.213309	1.0000	nonperiodic-templates
1	0	0	2	0	1	1	3	1	1	0.534146	1.0000	nonperiodic-templates
0	1	1	2	0	0	0	1	2	3	0.350485	1.0000	nonperiodic-templates
0	0	3	0	1	2	0	1	2	1	0.350485	1.0000	nonperiodic-templates
2	1	1	0	2	0	0	3	1	0	0.350485	1.0000	nonperiodic-templates
0	2	2	1	0	1	2	0	1	1	0.739918	1.0000	nonperiodic-templates
0	1	2	1	0	1	1	1	3	0	0.534146	1.0000	nonperiodic-templates
2	1	0	3	0	2	0	1	0	1	0.350485	1.0000	nonperiodic-templates
0	1	1	1	0	2	2	2	1	0	0.739918	1.0000	nonperiodic-templates
3	1	0	0	0	2	0	1	3	0	0.122325	0.9000 *	nonperiodic-templates
2	4	0	1	0	1	1	0	0	1	0.122325	0.9000 *	nonperiodic-templates
0	0	2	3	1	1	1	1	1	0	0.534146	1.0000	nonperiodic-templates
2	2	0	3	0	0	0	1	2	0	0.213309	1.0000	nonperiodic-templates
0	1	0	2	1	1	0	2	2	1	0.739918	1.0000	nonperiodic-templates
1	1	2	1	0	0	1	2	2	0	0.739918	1.0000	nonperiodic-templates
1	1	1	2	0	0	1	1	1	2	0.911413	1.0000	nonperiodic-templates
3	2	0	0	1	1	1	1	0	1	0.534146	0.9000 *	nonperiodic-templates
0 2	0	2	1	0	2	2	0	1 2	2	0.534146	1.0000	nonperiodic-templates
_	U	Τ	Τ	0	2	_	U	۷	0	0.534146	1.0000	nonperiodic-templates

0	0	1	2	1	3	1	1	1	0	0.534146	1.0000	nonperiodic-templates
0	1	0	1	1	1	0	1	2	3	0.534146	1.0000	nonperiodic-templates
0	1	2	0	0	1	1	1	3	1	0.534146	1.0000	nonperiodic-templates
2	0	0	1	3	1	2	0	1	0	0.350485	0.9000 *	nonperiodic-templates
0	0	1	1	2	1	1	0	3	1	0.534146	1.0000	nonperiodic-templates
0	1	0	2	0	5	0	0	1	1	0.008879	1.0000	nonperiodic-templates
1	1	0	1	1	0	0	2	3	1	0.534146	1.0000	nonperiodic-templates
0	0	1	2	0	2	0	1	3	1	0.350485	1.0000	nonperiodic-templates
1	2 1	0	0 2	0 1	3 1	1	2 3	0 1	1	0.350485 0.534146	1.0000	nonperiodic-templates
1	0	0	0	2	1	0	3	2	1	0.350485	0.9000 *	nonperiodic-templates nonperiodic-templates
1	3	0	2	1	1	0	1	1	0	0.534146	1.0000	nonperiodic-templates
1	1	1	0	2	2	0	2	1	0	0.739918	1.0000	nonperiodic-templates
1	1	1	0	0	1	2	3	1	0	0.534146	0.9000 *	nonperiodic-templates
0	2	0	3	1	0	1	1	2	0	0.350485	1.0000	nonperiodic-templates
0	1	1	1	0	3	1	0	2	1	0.534146	1.0000	nonperiodic-templates
1	0	0	1	0	2	0	4	0	2	0.066882	1.0000	nonperiodic-templates
1 2	1 2	3 0	0	2	2 1	0 1	0	1 3	0 1	0.350485 0.350485	0.9000 * 1.0000	nonperiodic-templates nonperiodic-templates
2	2	1	1	0	2	0	1	1	0	0.739918	1.0000	nonperiodic-templates
3	0	0	0	0	5	0	2	0	0	0.000954	1.0000	nonperiodic-templates
2	1	0	1	0	0	0	3	2	1	0.350485	0.9000 *	nonperiodic-templates
2	3	0	0	0	0	0	2	3	0	0.066882	1.0000	nonperiodic-templates
1	0	1	0	1	2	1	0	3	1	0.534146	1.0000	nonperiodic-templates
1	2	1	0	1	1	0	2	1	1	0.911413	1.0000	nonperiodic-templates
3	1	0	1 1	0	1 2	0	2 1	1 1	1	0.534146 0.739918	0.9000 *	nonperiodic-templates
0 1	2	1 2	1	0	4	2	0	2	0	0.739918	1.0000	nonperiodic-templates nonperiodic-templates
1	1	2	1	0	0	0	0	4	1	0.122325	1.0000	nonperiodic-templates
0	0	1	1	2	2	0	1	1	2	0.739918	1.0000	nonperiodic-templates
2	1	0	1	0	0	1	1	2	2	0.739918	1.0000	nonperiodic-templates
0	3	2	1	1	2	0	0	0	1	0.350485	1.0000	nonperiodic-templates
1	0	2	0	2	1	1	2	1	0	0.739918	1.0000	nonperiodic-templates
1	1 0	1 0	0	0	1 5	1	0 1	3 0	2	0.534146 0.002043	1.0000 0.9000 *	nonperiodic-templates
1	0	1	2	0	2	0	2	2	0	0.534146	1.0000	nonperiodic-templates nonperiodic-templates
1	3	1	1	0	2	1	0	1	0	0.534146	1.0000	nonperiodic-templates
1	1	1	1	1	0	0	0	2	3	0.534146	1.0000	nonperiodic-templates
1	0	0	0	0	3	0	3	2	1	0.122325	0.9000 *	nonperiodic-templates
0	0	2	1	0	1	1	3	1	1	0.534146	1.0000	nonperiodic-templates
2	1	1	1	1	2	0	0	1	1	0.911413	1.0000	nonperiodic-templates
0 1	0	1 2	0 1	0	2	1	2	3 1	1	0.350485 0.739918	1.0000	nonperiodic-templates nonperiodic-templates
2	1	1	0	0	0	0	1	1	4	0.122325	1.0000	nonperiodic-templates
1	2	1	0	0	1	1	2	2	0	0.739918	1.0000	nonperiodic-templates
0	1	1	1	1	2	1	3	0	0	0.534146	1.0000	nonperiodic-templates
2	1	2	0	1	0	0	2	1	1	0.739918	1.0000	nonperiodic-templates
1	0	0	1	1	2	1	0	3	1	0.534146	1.0000	nonperiodic-templates
1	2	1	0	0	2	1	2	1		0.739918	1.0000	nonperiodic-templates
1	1	1 0	0 1	0 1	2	0 1	1 1	2 1	2	0.739918 0.739918	1.0000	nonperiodic-templates nonperiodic-templates
0	0	3	2	1	2	1	0	1	0	0.350485	1.0000	nonperiodic-templates
3	2	1	0	0	1	0	2	1	0	0.350485	0.9000 *	nonperiodic-templates
1	1	3	0	0	1	0	1	2	1	0.534146	1.0000	nonperiodic-templates
2	2	0	1	0	2	0	2	0	1	0.534146	0.8000 *	nonperiodic-templates
1	1	0	0	0	6	1	0	1	0	0.000439	1.0000	nonperiodic-templates
2	0	1	0	1	1	2	2	1	0	0.739918	1.0000	nonperiodic-templates
1 2	1 2	1 1	1	1	0 2	1	1 2	3 0	0 1	0.739918 0.534146	1.0000	nonperiodic-templates nonperiodic-templates
2	1	0	1	1	1	0	2	2	0	0.739918	1.0000	nonperiodic-templates
1	3	1	0	0	1	0	2	1	1	0.534146	1.0000	nonperiodic-templates
2	1	2	1	1	2	0	0	0	1	0.739918	0.9000 *	nonperiodic-templates
0	0	0	0	0	3	2	2	1	2	0.213309	1.0000	nonperiodic-templates
1	0	1	0	3	2	0	0	2	1	0.350485	0.9000 *	nonperiodic-templates
0	1	0	1	1	3	0	2	1	1	0.534146	1.0000	nonperiodic-templates
2 1	0 1	3 0	0	1 2	0 2	2	0 1	2	0 1	0.213309 0.739918	1.0000	nonperiodic-templates nonperiodic-templates
1	0	4	1	1	2	0	0	0	1	0.122325	1.0000	nonperiodic-templates
2	0	1	0	1	0	1	2	3	0	0.350485	1.0000	nonperiodic-templates
0	0	2	1	0	2	0	1	4	0	0.066882	1.0000	nonperiodic-templates
0	2	1	0	0	2	0	2	0	3	0.213309	1.0000	nonperiodic-templates

1	1	2.	0	0	1	0	3	2	0	0.350485	0.9000 *	nonperiodic-templates
0	1	2	1	0	3	0	2	1	0	0.350485	1.0000	nonperiodic-templates
1	0	0	0	1	2	1	2	3	0	0.350485	0.9000 *	nonperiodic-templates
2	2	0	0	1	3	0	0	2	0	0.213309	0.9000 *	
0	3	1	1	1	2	1	0	1	0	0.534146	1.0000	nonperiodic-templates
1	2	0	0	1	1	2	1	1	1	0.911413	1.0000	nonperiodic-templates
1	1	1	1	0	2	0	1	0	3	0.534146	1.0000	nonperiodic-templates
1	0	0	0	0	3	1	1	2	2	0.350485	1.0000	nonperiodic-templates
1	0	0	1	0	0	1	4	3	0	0.035174	1.0000	nonperiodic-templates
2	0	1	0	2	0	1	2	1	1	0.739918	1.0000	nonperiodic-templates
0	0	0	0	2	1	3	1	2	1	0.350485	1.0000	nonperiodic-templates
1	1	0	1	0	1	0	3	3	0	0.213309	1.0000	nonperiodic-templates
0	2	0	0	1	3	0	3	0	1	0.122325	1.0000	nonperiodic-templates
1	1	1	1	2	1	1	0	2	0	0.911413	1.0000	nonperiodic-templates
3	3	0	0	0	2	0	1	1	0	0.122325	0.9000 *	nonperiodic-templates
2	0	1	0	1	2	0	0	2	2	0.534146	1.0000	nonperiodic-templates
2	2	0	2	0	1	1	2	0	0	0.534146	1.0000	nonperiodic-templates
3	1	1	0	0	0	0	1	3	1	0.213309	0.9000 *	nonperiodic-templates
1	0	3	0	0	3	0	1	0	2	0.122325	1.0000	nonperiodic-templates
1	2	1	1	2	0	0	2	1	0	0.739918	1.0000	nonperiodic-templates
1	3	0	1	0	3	0	1	1	0	0.213309	1.0000	nonperiodic-templates
2	1	2	1	0	2	0	0	0	2	0.534146	1.0000	nonperiodic-templates
0	2	1	1	0	2	1	1	2	0	0.739918	1.0000	nonperiodic-templates
1	1	0	0	0	1	1	1	2	3	0.534146	0.9000 *	nonperiodic-templates
2	1	1	0	1	1	0	0	4	0	0.122325	1.0000	nonperiodic-templates
1	2	1	0	1	2	0	2	1	0	0.739918	1.0000	apen
3	1	1	0	0	1	1	0	1	2	0.534146	1.0000	serial
3	0	1	1	2	0	1	0	1	1	0.534146	0.9000 *	serial

10nsc_50psf_24jrfout_lq_XORed.txt

(10ns system clk $\frac{1}{2}$ cycle, 50 ps difference in frequency, 24 ps jitter zone sampled on the rising edge and falling edge for data sets 1 through q and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
1	0	1	2	0	0	3	1	2	0	0.350485	1.0000	frequency
2	3	1	0	1	1	0	1	1	0	0.534146	1.0000	block-frequency
1	0	0	3	0	1	1	2	2	0	0.350485	1.0000	cumulative-sums
1	1	0	1	2	2	1	1	0	1	0.911413	1.0000	cumulative-sums
0	1	1	0	2	0	1	2	1	2	0.739918	1.0000	runs
1	0	1	1	5	0	1	0	1	0	0.017912	1.0000	fft
3	0	0	1	3	2	1	0	0	0	0.122325	0.8000 *	nonperiodic-templates
3	1 2	1	1	3 2	0	1	0 1	0	0	0.213309	1.0000	nonperiodic-templates
1	0	0	2	1	0 1	0	1	3	1 2	0.350485 0.350485	1.0000	nonperiodic-templates
2	1	2	1	2	1	0	0	1	0	0.739918	1.0000 1.0000	nonperiodic-templates nonperiodic-templates
2	1	0	1	0	2	1	1	0	2	0.739918	1.0000	nonperiodic-templates
1	1	1	0	2	0	0	3	2	0	0.739910	1.0000	nonperiodic-templates
1	1	1	2	0	1	0	2	0	2	0.739918	1.0000	nonperiodic-templates
4	0	3	0	1	0	0	1	1	0	0.035174	1.0000	nonperiodic-templates
1	1	2	1	0	1	1	0	2	1	0.911413	1.0000	nonperiodic-templates
0	2	1	1	1	0	2	2	1	0	0.739918	1.0000	nonperiodic-templates
1	2	1	0	1	1	1	2	0	1	0.911413	1.0000	nonperiodic-templates
2	2	2	0	0	0	1	1	2	0	0.534146	1.0000	nonperiodic-templates
1	1	1	1	0	0	2	1	1	2	0.911413	1.0000	nonperiodic-templates
1	0	1	1	2	0	2	1	2	0	0.739918	1.0000	nonperiodic-templates
2	2	1	1	0	1	0	2	0	1	0.739918	1.0000	nonperiodic-templates
1	1	3	0	0	1	0	2	2	0	0.350485	1.0000	nonperiodic-templates
0	2	2	1	0	1	0	1	1	2	0.739918	1.0000	nonperiodic-templates
2	0	0	1	1	3	0	1	1	1	0.534146	0.9000 *	nonperiodic-templates
0	0	0	2	1	2	0	2	2	1	0.534146	1.0000	nonperiodic-templates
0	2	3	0	2	0	1	1	1	0	0.350485	1.0000	nonperiodic-templates
3	0	1	2	2	0	0	0	1	1	0.350485	0.9000 *	nonperiodic-templates
0	1	1	2	0	1	2	1	0	2	0.739918	1.0000	nonperiodic-templates
1	2	0	1	0	3	1	1	1	0	0.534146	1.0000	nonperiodic-templates
2	1	0	1	2	0	2	2	0	0	0.534146	0.9000 *	nonperiodic-templates
2	4	1	2	0	0	1	0	0	0	0.066882	1.0000	nonperiodic-templates
1	1	0	4	1	1	0	0	1	1	0.213309	1.0000	nonperiodic-templates
0	1	1	1	2	2	1	0	2	0	0.739918	1.0000	nonperiodic-templates
1	0	3	2	1	0	0	0	2	1	0.350485	1.0000	nonperiodic-templates
3	0	0 2	1	2	0	0 2	2	0	2	0.213309	0.9000 *	nonperiodic-templates
2	1	1	0	1	1	2	1	1	0 1	0.534146 0.911413	1.0000	nonperiodic-templates
1	0	1	3	1	0	1	1	1	1	0.739918	1.0000	nonperiodic-templates nonperiodic-templates
2	3	1	0	0	1	1	1	0	1	0.733316	0.9000 *	nonperiodic-templates
0	0	2	1	3	0	0	1	2	1	0.350485	1.0000	nonperiodic-templates
0	0	2	1	0	1	3	1	1	1	0.534146	1.0000	nonperiodic-templates
1	1	0	1	0	1	1	3	0	2	0.534146	1.0000	nonperiodic-templates
0	1	0	2	0	1	2	0	4	0	0.066882	1.0000	nonperiodic-templates
2	1	1	1	2	0	1	1	0	1	0.911413	1.0000	nonperiodic-templates
1	0	1	0	2	3	2	1	0	0	0.350485	1.0000	nonperiodic-templates
2	0	0	0	0	1	1	2	2	2	0.534146	1.0000	nonperiodic-templates
2	3	1	2	1	1	0	0	0	0	0.350485	1.0000	nonperiodic-templates
1	0	0	1	0	2	3	0	2	1	0.350485	1.0000	nonperiodic-templates
1	1	1	3	0	1	1	1	0	1	0.739918	1.0000	nonperiodic-templates
1	2	1	0	1	0	0	1	3	1	0.534146	1.0000	nonperiodic-templates
1	1	1	0	0	0	2	2	2	1	0.739918	1.0000	nonperiodic-templates
2	0	0	2	1	1	1	1	0	2	0.739918	1.0000	nonperiodic-templates
0	2	1	2	1	0	2	1	1	0	0.739918	1.0000	nonperiodic-templates
2	1	0	0	3	1	0	1	2	0	0.350485	1.0000	nonperiodic-templates
1	0	0	1	4	1	1	1	1	0	0.213309	1.0000	nonperiodic-templates

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0	1	0	1	0	2	3	1	1	1	0.534146	1.0000		nonperiodic-templates
2	0	0	0	1	0	3	4	0	0	0.017912	0.8000	*	nonperiodic-templates
1	1	0	1	1	2	0	1	1	2	0.911413	0.9000		nonperiodic-templates
0	1	0	1	3	1	2	0	2	0	0.350485	1.0000		nonperiodic-templates
1	1	2	1	0	1	1	1	1	1	0.991468	1.0000		nonperiodic-templates
2	0	0	0	3	0	0	2	3	0	0.066882	0.9000	*	nonperiodic-templates
1	2.	0	0	2	0	2	0	3	0	0.213309	1.0000		nonperiodic-templates
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0	1	2	1	1	1	2	1	0	1	0.911413	1.0000		nonperiodic-templates
2	1	1	1	0	1	2	0	1	1	0.911413	0.9000	*	nonperiodic-templates
2	3	0	2	0	1	0	0	1	1	0.350485	1.0000		nonperiodic-templates
3	2	1	1	0	1	1	0	0	1	0.534146	1.0000		nonperiodic-templates
0	2	0	1	1	1	2	2	1	0	0.739918	1.0000		nonperiodic-templates
3	0	0	1	3	2	1	0	0	0	0.122325	0.8000	*	nonperiodic-templates
1	0	0	2	1	0	1	0	3	2	0.350485	1.0000		nonperiodic-templates
1	1	1	3	1	0	0	0	2	1	0.534146	1.0000		nonperiodic-templates
1	2	1	1	0	0	1	3	0	1	0.534146	1.0000		nonperiodic-templates
1	1	0	0	0	2	3	2	1	0	0.350485	1.0000		nonperiodic-templates
1	2	0	1	2	0	2	0	2	0	0.534146	1.0000		nonperiodic-templates
3	1	1	0	1	0	1	2	0	1	0.534146	1.0000		apen
2	0	3	0	1	2	1	0	0	1	0.350485	0.9000	*	serial
1	1	2	1	1	2	1	1	0	0	0.911413	0.9000	*	serial

provided in the addendum section of the documentation.

For further guidelines construct a probability table using the MAPLE program

10nsc_100psf_24jrfout_afX

(10ns system clk $\frac{1}{2}$ cycle, 100 ps difference in frequency, 24 ps jitter zone sampled on the rising edge and falling edge for data sets a through f and consecutive outputs Xored)

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 P-VALUE PROPORTION STATISTICAL TEST 3 1 2 0 1 1 1 0 0 1 1 0 0.534146 1.0000 frequency 1 1 1 2 1 1 2 0 0 1 1 0 0.534146 1.0000 cumulative-sums 2 1 1 1 1 1 1 1 0 1 2 0 0.911413 1.0000 cumulative-sums 3 2 1 0 0 1 1 0 1 1 1 1 1 0.534146 1.0000 cumulative-sums 6 0 0 1 2 0 0 3 1 2 1 0.534146 1.0000 frequency 8 1 0 0 1 2 0 0 3 1 2 1 0.534146 1.0000 cumulative-sums 9 1 0 0 1 2 0 0 3 1 2 1 0.534146 1.0000 cumulative-sums 1 0 0 2 5 1 0 1 1 0 1 0 0.008879 1.0000 frequency 1 1 0 0 1 2 0 0 3 1 2 1 0.534146 1.0000 cumulative-sums 2 0 1 1 0 0 1 3 1 1 0.534146 1.0000 cumulative-sums 2 0 1 1 0 0 0 3 1 2 1 0.534146 1.0000 cumulative-sums 1 0 0 2 0 2 2 2 0 0 0 0.55485 1.0000 cumulative-sums 1 0 0 1 0 2 0 2 1 0 1 0 1 0 0.008879 1.0000 cumulative-sums 2 0 1 1 0 0 1 3 1 1 0.534146 1.0000 cumperiodic-templates 1 0 0 0 1 0 2 2 1 0 3 0.55485 1.0000 cumperiodic-templates 1 0 0 0 1 0 2 2 1 1 0 3 0.55485 1.0000 cumperiodic-templates 2 1 0 0 1 1 0 2 2 1 1 1 1 0 0.911413 1.0000 cumperiodic-templates 2 1 0 2 0 0 0 1 2 0.534146 1.0000 cumperiodic-templates 2 1 0 2 0 0 0 1 2 0 0.534146 1.0000 cumperiodic-templates 3 1 1 0 0 0 1 1 3 3 0 0.213309 1.0000 cumperiodic-templates 3 1 1 0 0 0 1 1 3 3 0 0.213309 1.0000 cumperiodic-templates 3 1 1 0 0 0 1 1 3 3 0 0.213309 1.0000 cumperiodic-templates 3 1 1 0 0 0 0 1 1 3 3 0 0.213309 1.0000 cumperiodic-templates 4 1 0 0 1 0 4 0 0 2 0 0.666882 0.9000 * nonperiodic-templates 5 1 0 0 1 0 2 0 1 2 1 1 0 0.13309 1.0000 cumperiodic-templates 6 1 1 0 1 1 2 1 2 1 1 1 1 0.911413 1.0000 cumperiodic-templates 6 1 1 0 1 1 2 1 2 1 1 1 1 0.911413 1.0000 cumperiodic-templates 7 1 0 0 1 1 2 2 1 0 1 1 0.91413 1.0000 cumperiodic-templates 8 1 1 0 0 0 0 1 1 2 2 1 0 1 1 0.91413 1.0000 cumperiodic-templates 9 1 1 0 0 0 1 0 4 0 0 2 0 0.666882 0.9000 * nonperiodic-templates 1 1 0 0 0 1 0 1 0 4 0 0 0.23309 1.0000 cumperiodic-templates 1 1 0 0 0 0 1 1 2 2 1 0 0 1 1 0.91413 1.0000 cumperiodic-templates 1 1 0 0 0 0 1 1 2 2 1 0 0 1 1 0.91413 1.0000 cumperiodic-templates 1 1 0 0 0 0 1 1 2 0 1 0 0 0.330													
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3	1	1	1	2	1	1	2	0	0	1	0.911413	1.0000	block-frequency
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1 1 1 0 1 2 0 3 0 1 0.534146 1.0000 nonperiodic-templates	0	1	0	1	1	4	0	2	1	0			
	0	0	0	1	1	2	2	3	1	0	0.350485	1.0000	
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	1	0	1	2	2	2	1	1	0	0	0.739918	0.9000 *	nonperiodic-templates

0	1	0	1	2	0	0	2	1	3	0.350485	1.0000		nonperiodic-templates
3	2	2	0	0	1	1	1	0	0	0.350485	1.0000		nonperiodic-templates
1	0	2	0	0	1	0	2	3	1	0.350485	0.9000	*	nonperiodic-templates
0	2	3	0	2	0	3	0	0	0	0.066882	1.0000		nonperiodic-templates
2	1	1	1	0	1	1	2	0	1	0.911413	1.0000		nonperiodic-templates
3	0	0	1	0	0	1 2	2	1 2	2	0.350485	1.0000		nonperiodic-templates
1 0	0 1	1	1	1 1	0 4	1	2	1	0	0.911413 0.122325	1.0000		nonperiodic-templates
3	0	0	0	0	1	2	2	2	0	0.122323	1.0000		nonperiodic-templates nonperiodic-templates
1	2	1	0	2	1	1	1	0	1	0.911413	1.0000		nonperiodic-templates
1	1	1	0	2	2	0	0	0	3	0.350485	0.9000	*	nonperiodic-templates
1	0	0	0	0	1	2	2	3	1	0.350485	1.0000		nonperiodic-templates
2	2	0	3	2	0	0	0	1	0	0.213309	1.0000		nonperiodic-templates
3	2	1	0	1	0	1	0	1	1	0.534146	1.0000		nonperiodic-templates
1	0	2	0	0	1	2	1	2	1	0.739918	1.0000		nonperiodic-templates
0	0	2	1	1	1	2	2	1	0	0.739918	1.0000		nonperiodic-templates
1	2	0	0	0	2	3	0	2	0	0.213309	1.0000		nonperiodic-templates
1 1	0	1 1	3 2	2	0 1	0	1 3	1 1	1	0.534146 0.534146	1.0000		nonperiodic-templates nonperiodic-templates
1	0	2	3	1	1	1	1	0	0	0.534146	1.0000		nonperiodic-templates
0	0	1	2	0	2	2	1	1	1	0.739918	1.0000		nonperiodic-templates
1	0	1	2	0	2	1	1	0	2	0.739918	0.9000	*	nonperiodic-templates
0	0	1	1	0	3	0	4	1	0	0.035174	1.0000		nonperiodic-templates
0	0	0	2	1	1	4	1	1	0	0.122325	1.0000		nonperiodic-templates
0	1	1	0	2	1	3	0	1	1	0.534146	1.0000		nonperiodic-templates
0	2	0	0	1	0	1	3	2	1	0.350485	1.0000		nonperiodic-templates
3	2	1	0	0	0	3	0	1	0	0.122325	0.9000		nonperiodic-templates
1	0	1	1	1	0	0	1	3	2	0.534146	0.9000	*	nonperiodic-templates
1	1	0	0	3	3	0	1	1	0	0.213309	1.0000	4	nonperiodic-templates
1 1	2	1 1	1	0 1	2	0 2	1	1 2	1 2	0.911413 0.739918	0.9000	^	nonperiodic-templates nonperiodic-templates
0	2	0	1	0	0	2	2	1	2	0.534146	1.0000		nonperiodic-templates
0	2	0	1	0	3	2	1	1	0	0.350485	1.0000		nonperiodic-templates
1	1	1	1	1	0	1	0	1	3	0.739918	1.0000		nonperiodic-templates
0	1	1	2	3	0	0	0	3	0	0.122325	1.0000		nonperiodic-templates
1	0	2	2	0	1	1	1	2	0	0.739918	1.0000		nonperiodic-templates
2	1	0	1	0	0	3	1	0	2	0.350485	1.0000		nonperiodic-templates
1	1	0	0	2	2	2	0	2	0	0.534146	0.9000	*	nonperiodic-templates
2	1	0	1	0	2	1	1	0	2	0.739918	1.0000		nonperiodic-templates
0	1 1	0	2	2 1	0	3 2	0	2 1	0 3	0.213309 0.350485	1.0000		nonperiodic-templates
0	0	2	2	2	0	0	2	0	2	0.350485	1.0000		nonperiodic-templates nonperiodic-templates
2	0	0	1	2	1	2	1	0	1	0.739918	1.0000		nonperiodic-templates
2	2	1	1	2	1	1	0	0	0	0.739918	0.9000	*	nonperiodic-templates
3	1	0	0	1	0	0	0	4	1	0.035174	1.0000		nonperiodic-templates
1	1	1	2	1	2	1	1	0	0	0.911413	0.9000	*	nonperiodic-templates
2	0	0	1	1	1	0	3	1	1	0.534146	1.0000		nonperiodic-templates
3	1	0	0	1	0	2	1	2	0	0.350485	0.9000	*	nonperiodic-templates
0	1	1	2	0	3	0	1	0	2	0.350485	1.0000		nonperiodic-templates
1	3 1	1	0 3	0	2 1	1 1	0 1	2 1	0	0.350485 0.739918	1.0000		nonperiodic-templates nonperiodic-templates
1	0	0	1	1	2	2	0	3	0	0.350485	1.0000		nonperiodic-templates
1	4	0	1	0	0	3	1	0	0	0.035174	1.0000		nonperiodic-templates
0	0	1	3	0	3	2	1	0	0	0.122325	1.0000		nonperiodic-templates
0	2	0	1	0	0	3	2	1	1	0.350485	1.0000		nonperiodic-templates
1	1	1	0	2	2	1	0	0	2	0.739918	1.0000		nonperiodic-templates
2	1	1	0	2	1	0	2	1	0	0.739918	1.0000		nonperiodic-templates
1	0	0	0	1	1	3	2	2	0	0.350485	1.0000		nonperiodic-templates
0	0	1	1	4	1	1	1	1	0	0.213309	1.0000		nonperiodic-templates
1 1	1 3	1	0 2	0	2	1 1	2 1	2	0 2	0.739918 0.350485	1.0000		nonperiodic-templates nonperiodic-templates
1	1	0	2	1	1	1	2	1	0	0.911413	1.0000		nonperiodic-templates
1	0	1	0	0	1	4	1	1	1	0.213309	1.0000		nonperiodic-templates
2	1	2	1	0	0	2	0	1	1	0.739918	1.0000		nonperiodic-templates
0	0	1	3	1	0	0	3	1	1	0.213309	1.0000		nonperiodic-templates
0	2	1	1	0	0	1	2	2	1	0.739918	1.0000		nonperiodic-templates
2	1	1	0	1	2	2	1	0	0	0.739918	1.0000		nonperiodic-templates
1	0	1	0	1 3	4	1	0	2	0	0.122325	0.9000	*	nonperiodic-templates
1 0	1	0 1	1 2	3 1	0 1	0 1	0 1	1 1	3 2	0.213309 0.911413	1.0000		nonperiodic-templates nonperiodic-templates
1	0	0	1	0	2	2	0	0	4	0.911413	0.9000	*	nonperiodic-templates nonperiodic-templates
_	U	U	_	U	_	_	U	U	-1	3.000002	0.000		berroare cembraces

1	0	0	1	0	2.	3	0	1	2.	0.350485	1.0000	nonperiodic-templates
0	0	0	3	1	2.	1	1	1	1	0.534146	1.0000	nonperiodic-templates
3	0	0	1	2	0	2.	0	2	0	0.213309	1.0000	nonperiodic-templates
1	3	0	1	1	2.	0	0	2	0	0.350485	1.0000	nonperiodic-templates
2.	0	2.	1	0	2	0	2.	1	0	0.534146	0.9000 *	
_	0	3	-	1	1	0	0	_	-	0.534146		nonperiodic-templates
0	2	-	0	_	_	•	~	0	3		1.0000	nonperiodic-templates
3	0	1	3	0	0	0	0	3	0	0.035174	0.9000 *	nonperiodic-templates
1	1	0	1	2	1	1	1	1	1	0.991468	0.9000 *	nonperiodic-templates
0	1	0	1	1	3	2	1	0	1	0.534146	1.0000	nonperiodic-templates
1	1	2	2	0	0	1	0	0	3	0.350485	1.0000	nonperiodic-templates
2	0	0	1	1	1	0	2	2	1	0.739918	1.0000	nonperiodic-templates
1	0	0	1	0	1	0	1	2	4	0.122325	0.9000 *	nonperiodic-templates
2	1	1	2	2	0	0	0	0	2	0.534146	0.9000 *	nonperiodic-templates
2	0	1	0	2	0	0	2	3	0	0.213309	1.0000	nonperiodic-templates
2	0	0	1	3	0	2	1	1	0	0.350485	1.0000	nonperiodic-templates
2	1	0	3	0	0	1	1	1	1	0.534146	1.0000	nonperiodic-templates
1	1	1	0	2	0	1	1	2	1	0.911413	1.0000	nonperiodic-templates
1	0	2.	0	2.	1	0	1	2.	1	0.739918	1.0000	nonperiodic-templates
1	1	1	2	1	3	1	0	0	0	0.534146	1.0000	nonperiodic-templates
0	0	2	1	0	0	3	1	2	1	0.350485	1.0000	nonperiodic-templates
1	0	0	3	2	1	0	2	1	0	0.350485	0.9000 *	nonperiodic-templates
1	1	1	0	2	0	3	0	2	0	0.350485	1.0000	nonperiodic-templates
0	0	0	2.	1	1	3	2	1	0	0.350485	1.0000	nonperiodic-templates
0	1	1	1	1	1	1	2.	1	1	0.991468	1.0000	nonperiodic-templates
1	1	0	2	3	1	1	1	_	0	0.534146	1.0000	
_	_	-	_	-	_	_	_	0	-			nonperiodic-templates
1	0	2	0	1	0	0	2	2	2	0.534146	1.0000	apen
1	1	0	0	0	1	1	2	1	3	0.534146	1.0000	serial
1	0	1	1	1	0	3	0	2	1	0.534146	1.0000	serial

(10ns system clk $\frac{1}{2}$ cycle, 100 ps difference in frequency, 24 ps jitter zone sampled on the rising edge and falling edge for data sets 1 through q and consecutive outputs Xored)

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	C6		C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
1	2	0	1	1	0	0	3	1	1	0.534146	1.0000	frequency
1	4	0	3	0	0	0	1	1	0	0.035174	1.0000	block-frequency
0	2	3	1	2	1	0	0	0	1	0.350485	1.0000	cumulative-sums
1	2	0	2	2	1	0	0	2	0	0.534146	1.0000	cumulative-sums
4	1	1	0	2	1	0	1	0	0	0.122325	1.0000	runs
0	0	0	0	3	1	0	1	5	0	0.002043	1.0000	fft
0	0	1	3	0	1	1	2	2	0	0.350485	1.0000	nonperiodic-templates
1	0	0	1	2	0	1	2	2	1	0.739918	1.0000	nonperiodic-templates
1 1	0	0 1	1	1 2	0	2	1 2	2	2	0.739918 0.739918	1.0000 0.9000 *	nonperiodic-templates nonperiodic-templates
0	1	0	3	1	0	1	1	1	2	0.739916	1.0000	nonperiodic-templates
0	0	1	2	1	1	4	1	0	0	0.122325	1.0000	nonperiodic-templates
2	0	1	0	0	1	2	1	1	2	0.739918	1.0000	nonperiodic-templates
0	0	2	0	1	2	2	1	2	0	0.534146	1.0000	nonperiodic-templates
1	0	2	1	0	2	1	2	0	1	0.739918	1.0000	nonperiodic-templates
0	0	2	0	2	1	0	3	1	1	0.350485	1.0000	nonperiodic-templates
0	2	0	0	2	1	2	2	1	0	0.534146	1.0000	nonperiodic-templates
0	0	1	1	1	2	1	0	2	2	0.739918	1.0000	nonperiodic-templates
1	0	1	2	1	1	3	0	1	0	0.534146	1.0000	nonperiodic-templates
3	1	1	0	0	0	1	2	1	1	0.534146	1.0000	nonperiodic-templates
1	0	0	0	1	3	0	0	2	3	0.122325	1.0000	nonperiodic-templates
3	3	0	0	0	0	0	1	3	0	0.035174	0.8000 *	nonperiodic-templates
1	2	0	2	0	3	0	1	1	0	0.350485	1.0000	nonperiodic-templates
1	0	3	2	1	0	2	0	1	0	0.350485	1.0000	nonperiodic-templates
0	0	2	0	0	1	2	3	1	1	0.350485	1.0000	nonperiodic-templates
1	0	1 2	1	1	0	1	0	2	3	0.534146	1.0000	nonperiodic-templates
4 1	0 1	1	0	1	0 2	2	1	0	0	0.066882	1.0000	nonperiodic-templates nonperiodic-templates
0	1	0	0	1	2	3	2	0	1	0.350485	1.0000	nonperiodic-templates
0	2	1	2	0	1	1	1	0	2	0.739918	1.0000	nonperiodic-templates
2	1	0	1	2	0	2	0	2	0	0.534146	1.0000	nonperiodic-templates
0	0	1	1	1	4	3	0	0	0	0.035174	1.0000	nonperiodic-templates
2	0	0	0	0	2	2	1	2	1	0.534146	0.9000 *	nonperiodic-templates
0	1	2	0	1	0	2	1	2	1	0.739918	1.0000	nonperiodic-templates
0	0	0	3	0	0	2	1	1	3	0.122325	1.0000	nonperiodic-templates
0	0	1	1	0	1	3	0	3	1	0.213309	1.0000	nonperiodic-templates
3	1	0	1	2	0	1	0	2	0	0.350485	0.9000 *	nonperiodic-templates
1	3	1	1	0	2	1	0	1	0	0.534146	1.0000	nonperiodic-templates
1	1	1	1	1	0	0	1	3	1	0.739918	1.0000	nonperiodic-templates
0	0	0	2	1	2	2	1	2	0	0.534146	1.0000	nonperiodic-templates
2	0	2	0	1	0	0	2	1	2	0.534146	0.9000 *	nonperiodic-templates
1 0	0	1 2	0	0	2	3 2	1	1	1	0.534146	0.9000 *	nonperiodic-templates
0	1	0	2	3	1	1	0	2	0	0.350485	1.0000	nonperiodic-templates nonperiodic-templates
0	0	0	0	1	2	2	2	1	2	0.534146	1.0000	nonperiodic-templates
2	0	0	2	0	0	0	4	2	0	0.035174	1.0000	nonperiodic-templates
2	1	1	2	1	0	2	0	1	0	0.739918	1.0000	nonperiodic-templates
1	1	2	0	0	1	1	1	3	0	0.534146	1.0000	nonperiodic-templates
3	1	1	1	0	1	1	0	2	0	0.534146	1.0000	nonperiodic-templates
2	2	0	0	1	0	2	3	0	0	0.213309		nonperiodic-templates
0	0	1	2	1	1	2	2	0	1	0.739918		nonperiodic-templates
3	0	1	3	0	1	0	1	1	0	0.213309		nonperiodic-templates
1	0	0	2	1	1	1	1	1	2	0.911413		nonperiodic-templates
0	0	2	0	2	2	2	1	1	0	0.534146	1.0000	nonperiodic-templates
1	0	0	0	2	2	4	1	0	0	0.066882		nonperiodic-templates
2	0	0	3	2	0	1	0	0	2	0.213309		nonperiodic-templates
3	1	1	0	0	0	2	1	0	2	0.350485		nonperiodic-templates
2	1	1	0	0	0	2	1	2	1	0.739918	0.9000 *	nonperiodic-templates

3	2	2	1	1	1	0	0	0	0	0.350485	0.9000	*	nonperiodic-templates
0	1	0	0	1	2	2	2	1	1	0.739918	1.0000		nonperiodic-templates
1	0	0	1	3	1	2	0	1	1	0.534146	1.0000		nonperiodic-templates
0	1	0	0	0	0	3	1	1	4	0.035174	1.0000		nonperiodic-templates
1	1	2	0	2	2	0	2	0	0	0.534146	1.0000		nonperiodic-templates
0	1	1	0	2	1	2	0	3	0	0.350485	1.0000		nonperiodic-templates
0	0	0	1	4	1	2	0	1	1	0.122325	1.0000		nonperiodic-templates
1	2	0	1	1	3	1	1	0	0	0.534146	1.0000		nonperiodic-templates
3	0	2	1	2	1	1	0	0	0	0.350485	0.9000	*	nonperiodic-templates
1	0	2	1	0	2	1	1	2	0	0.739918	1.0000		nonperiodic-templates
0	1	0	1	1	3	0	1	2	1	0.534146	1.0000		nonperiodic-templates
0	2	1	0	0	3	0	1	1	2	0.350485	1.0000	_	nonperiodic-templates
2	1 2	0	0	2	0	0	3	1 2	1	0.350485	0.9000		nonperiodic-templates
1 1	2	0	2	1	1 2	1	0 2	0	0	0.350485 0.534146	0.9000	^	nonperiodic-templates nonperiodic-templates
2	1	1	2	0	0	1	1	1	1	0.911413	1.0000		nonperiodic-templates
1	2	0	2	2	0	0	2	1	0	0.534146	0.9000	*	nonperiodic-templates
0	1	1	0	0	0	4	2	1	1	0.122325	1.0000		nonperiodic-templates
1	0	1	0	1	1	2	2	1	1	0.911413	1.0000		nonperiodic-templates
0	0	1	1	1	1	1	1	2	2	0.911413	1.0000		nonperiodic-templates
0	0	0	2	0	1	1	0	4	2	0.066882	1.0000		nonperiodic-templates
2	1	1	1	1	1	0	2	1	0	0.911413	0.9000	*	nonperiodic-templates
1	0	1	2	1	1	1	1	1	1	0.991468	1.0000		nonperiodic-templates
1	1	1	2	1	1	1	1	0	1	0.991468	1.0000		nonperiodic-templates
2	1	3	0	0	0	0	1	2	1	0.350485	1.0000		nonperiodic-templates
2	2	0	2	0	1	1	0	1	1	0.739918	1.0000		nonperiodic-templates
3	0	0	2	2	0	0	0	1	2	0.213309	0.9000	*	nonperiodic-templates
1	0	1	1	0	4	1	2	0	0	0.122325	1.0000		nonperiodic-templates
2	3	0	2	1	1	0	1	0	0	0.350485	1.0000		nonperiodic-templates
1	0	0	2	0	3	1	1	0	2	0.350485	1.0000		nonperiodic-templates
0 1	1	1	1	1	2	1 2	1	0 1	2	0.911413 0.350485	1.0000		nonperiodic-templates nonperiodic-templates
0	1	2	0	0	0	2	0	1	4	0.066882	1.0000		nonperiodic-templates
0	1	0	2	0	1	1	1	3	1	0.534146	1.0000		nonperiodic-templates
2	2	1	1	1	1	1	0	0	1	0.911413	1.0000		nonperiodic-templates
0	2	0	2	3	1	0	0	1	1	0.350485	1.0000		nonperiodic-templates
5	0	0	2	0	0	1	0	1	1	0.008879	0.9000	*	nonperiodic-templates
2	2	1	0	0	0	2	3	0	0	0.213309	1.0000		nonperiodic-templates
1	0	2	1	1	0	0	2	1	2	0.739918	1.0000		nonperiodic-templates
0	0	1	3	0	2	0	1	2	1	0.350485	1.0000		nonperiodic-templates
1	0	0	3	0	0	5	0	1	0	0.002043	1.0000		nonperiodic-templates
3	0	1	0	2	0	1	1	1	1	0.534146	1.0000		nonperiodic-templates
0	2	0	1	1	2	2	1	1	0	0.739918	1.0000		nonperiodic-templates
1	1	2	1	0	0	3	1	0	1	0.534146	1.0000		nonperiodic-templates
0	2	1	1	0	2	1	1	1	1	0.911413	1.0000		nonperiodic-templates
0	2	2 2	1 3	1 2	1	1	0 2	0 1	2	0.739918 0.213309	1.0000		nonperiodic-templates nonperiodic-templates
0	0	2	0	2	1	2	2	1	0	0.534146	1.0000		nonperiodic-templates
1	0	1	2	1	0	1	1	2	1	0.911413	1.0000		nonperiodic-templates
1	0	0	1	1	2	2	1	0	2	0.739918	1.0000		nonperiodic-templates
1	1	0	0	0	2	2	1	3	0	0.350485	1.0000		nonperiodic-templates
1	1	2	3	0	0	0	2	0	1	0.350485	1.0000		nonperiodic-templates
1	2	1	2	1	2	0	0	1	0	0.739918	1.0000		nonperiodic-templates
1	0	4	1	2	0	1	0	1	0	0.122325	1.0000		nonperiodic-templates
1	2	3	0	0	1	1	0	2	0	0.350485	1.0000		nonperiodic-templates
0	2	0	1	4	0	2	1	0	0	0.066882	1.0000		nonperiodic-templates
1	0	2	1	2	0	2	0	2	0	0.534146	1.0000		nonperiodic-templates
0	1	0	1	0	1	2	3	2	0	0.350485	1.0000		nonperiodic-templates
0	3	0	3	0	1	2	0	1	0	0.122325	1.0000		nonperiodic-templates
0	1	1	2	1	0	0	2	2	1	0.739918	1.0000		nonperiodic-templates
2	3 0	0	0	0 1	2	3 4	0 1	0 2	0	0.066882 0.066882	1.0000		nonperiodic-templates nonperiodic-templates
0	2	2	0	0	2	2	0	1	1	0.000882	1.0000		nonperiodic-templates
0	0	1	1	1	1	1	2	2	1	0.911413	1.0000		nonperiodic-templates
1	0	1	1	0	2	4	1	0	0	0.122325	1.0000		nonperiodic-templates
0	1	1	4	0	0	0	1	2	1	0.122325	1.0000		nonperiodic-templates
3	1	0	2	0	0	2	0	1	1	0.350485	0.9000	*	nonperiodic-templates
0	0	0	3	2	2	1	1	1	0	0.350485	1.0000		nonperiodic-templates
1	1	1	2	0	3	1	1	0	0	0.534146	1.0000		nonperiodic-templates
0	2	1	1	1	0	0	3	2	0	0.350485	1.0000		nonperiodic-templates
0	1	0	3	0	2	1	0	3	0	0.122325	1.0000		nonperiodic-templates

0	Ο	2	2	0	0	0	5	0	1	0.004301	1.0000	nonperiodic-templates
1	2	1	3	0	0	0	2.	0	1	0.350485	0.9000 *	nonperiodic-templates
0	1	1	1	2	0	2	2.	1	0	0.739918	1.0000	nonperiodic-templates
2.	2	1	0	0	1	1	2.	0	1	0.739918	0.9000 *	nonperiodic-templates
0	2	2	0	1	1	0	2.	1	1	0.739918	1.0000	
0	2	0	1	0	1	1	1	3	1	0.739918	1.0000	nonperiodic-templates
•	_	0	_	2	_	1	2.	-	_			nonperiodic-templates
2	0	0	2	_	0	_	_	0	1	0.534146	1.0000	nonperiodic-templates
3	2	0	1	0	0	1	0	2	1	0.350485	1.0000	nonperiodic-templates
1	0	2	1	0	1	2	0	3	0	0.350485	1.0000	nonperiodic-templates
1	2	0	1	1	1	1	2	1	0	0.911413	0.9000 *	nonperiodic-templates
3	0	1	0	0	1	1	2	1	1	0.534146	1.0000	nonperiodic-templates
0	1	0	0	2	1	2	1	2	1	0.739918	1.0000	nonperiodic-templates
1	1	2	0	0	1	1	1	2	1	0.911413	1.0000	nonperiodic-templates
0	1	1	0	2	1	1	2	1	1	0.911413	1.0000	nonperiodic-templates
2	0	1	0	2	1	1	1	2	0	0.739918	1.0000	nonperiodic-templates
0	2	2	1	0	1	1	2	0	1	0.739918	1.0000	nonperiodic-templates
0	0	1	1	1	3	1	1	0	2	0.534146	1.0000	nonperiodic-templates
2	0	1	0	1	1	0	3	1	1	0.534146	1.0000	nonperiodic-templates
0	2	2	0	1	2	0	3	0	0	0.213309	1.0000	nonperiodic-templates
0	0	1	3	0	1	1	2	2	0	0.350485	1.0000	nonperiodic-templates
2.	0	1	1	0	1	2.	1	1	1	0.911413	0.9000 *	nonperiodic-templates
0	0	1	0	2	3	1	3	0	0	0.122325	1.0000	nonperiodic-templates
0	0	1	1	1	2.	3	0	1	1	0.534146	1.0000	nonperiodic-templates
0	2	1	1	2	1	1	0	1	1	0.911413	1.0000	nonperiodic-templates
0	0	0	1	0	1	0	1	5	2	0.008879	1.0000	nonperiodic-templates
3	3	0	1	0	1	0	0	0	2	0.122325	1.0000	apen
2	2	0	1	1	1	0	0	2	1	0.739918	1.0000	serial
1	1	1	1	1	1	1	0	2.	_	0.739918		
1	Т	Τ	1	Τ	1	Τ	U	2	1	0.991468	1.0000	serial

(10ns system clk $\frac{1}{2}$ cycle, 120 ps difference in frequency, 24 ps jitter zone sampled on the rising and falling edge for data sets a through f and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
7	2	0	1	0	0	0	0	0	0	0.000001	* 0.4000 *	frequency
3	4	1	1	0	0	0	1	0	0	0.035174	0.9000 *	block-frequency
8	1	0	0	0	1	0	0	0	0	0.000000		cumulative-sums
7	2	0	0	1	0	0	0	0	0	0.000001		cumulative-sums
2	0	3	0	0	1	1	0	0	3	0.122325	0.9000 *	runs
0	2	0	1	1	0	1	1	4	0	0.122325	1.0000	fft
0	0	1	2	3	1	1	1	0	1	0.534146	1.0000	nonperiodic-templates
0	0	2	2	2	1	2	0	0	1	0.534146	1.0000	nonperiodic-templates
2	0	2	1	0 1	1	1	1	2	0	0.739918	1.0000	nonperiodic-templates nonperiodic-templates
0	0	1	1	2	0	0	1	3	2	0.350485	1.0000	=
0	0	0	1	2	2	2	3	0	0	0.213309	1.0000	nonperiodic-templates nonperiodic-templates
1	2	1	2	0	1	1	1	0	1	0.911413	1.0000	nonperiodic-templates
0	0	1	1	2	1	1	2	2	0	0.739918	1.0000	nonperiodic-templates
0	0	2	0	1	1	1	2	1	2	0.739918	1.0000	nonperiodic-templates
0	2	0	3	0	2	1	0	2	0	0.213309	1.0000	nonperiodic-templates
2	0	2	0	0	1	2	2	1	0	0.534146	0.9000 *	nonperiodic-templates
1	0	1	1	1	2	1	1	2	0	0.911413	1.0000	nonperiodic-templates
0	1	2	1	0	1	1	0	4	0	0.122325	1.0000	nonperiodic-templates
1	1	1	1	1	0	1	1	1	2	0.991468	1.0000	nonperiodic-templates
1	1	1	3	0	1	1	1	0	1	0.739918	0.9000 *	nonperiodic-templates
1	2	1	2	0	0	1	1	1	1	0.911413	1.0000	nonperiodic-templates
0	2	1	0	0	0	2	1	1	3	0.350485	1.0000	nonperiodic-templates
0	0	2	0	3	1	1	1	1	1	0.534146	1.0000	nonperiodic-templates
1	0	0	2	0	0	2	1	1	3	0.350485	1.0000	nonperiodic-templates
0	0	1	0	2	2	1	2	1	1	0.739918	1.0000	nonperiodic-templates
2	0	2	1	1	0	0	1	0	3	0.350485	0.9000 *	nonperiodic-templates
1	3	1	1	1	1	1	1	0	0	0.739918	0.9000 *	nonperiodic-templates
1	0	4	0	1	1	1	1	1	0	0.213309	1.0000	nonperiodic-templates
2	0	1	1	1	1	2	0	1	1	0.911413	1.0000	nonperiodic-templates
0	3	0	1	0	2	1	2	0	1	0.350485	1.0000	nonperiodic-templates
2	1	2	0	0	1	1	0	1	2	0.739918	0.9000 *	nonperiodic-templates
1	1	0	1	1	0	3	2	0	1	0.534146	1.0000	nonperiodic-templates
2	1	1 1	0 3	0	1	2	1	1	1 2	0.911413 0.213309	1.0000	nonperiodic-templates
0	0	1	0	1	1	2	2	2	1	0.739918	0.9000 * 1.0000	nonperiodic-templates nonperiodic-templates
2	1	0	1	2	0	2	1	1	0	0.739918	1.0000	nonperiodic-templates
0	1	0	1	4	0	1	0	1	2	0.122325	1.0000	nonperiodic-templates
2	0	0	0	2	2	1	0	1	2	0.534146	0.9000 *	nonperiodic-templates
0	0	0	4	0	0	1	0	2	3	0.017912	1.0000	nonperiodic-templates
1	1	1	2	0	0	0	1	2	2	0.739918	1.0000	nonperiodic-templates
1	0	0	2	0	1	2	1	1	2	0.739918	1.0000	nonperiodic-templates
2	0	2	0	0	4	0	1	0	1	0.066882	1.0000	nonperiodic-templates
0	0	2	0	0	2	0	3	1	2	0.213309	1.0000	nonperiodic-templates
0	2	1	1	1	3	1	1	0	0	0.534146	1.0000	nonperiodic-templates
1	0	0	0	1	3	1	0	1	3	0.213309	1.0000	nonperiodic-templates
3	3	0	1	0	0	2	1	0	0	0.122325	0.9000 *	nonperiodic-templates
1	0	1	1	1	1	2	1	1	1	0.991468	1.0000	nonperiodic-templates
0	1	0	0	2	2	2	0	2	1	0.534146	1.0000	nonperiodic-templates
0	3	0	1	1	1	1	2	0	1	0.534146	1.0000	nonperiodic-templates
0	2	3	0	1	0	0	2	1	1	0.350485	1.0000	nonperiodic-templates
0	1	0	1	2	0	1	1	3	1	0.534146	1.0000	nonperiodic-templates
0	1	0	1	2	2	0	1	0	3	0.350485	1.0000	nonperiodic-templates
0	1	1	1	0	0	3	1	0	3	0.213309	1.0000	nonperiodic-templates
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1	0	1	0	2	0	2	1	2	1	0.739918	1.0000	nonperiodic-templates
1	3	2	0	0	0	0	3	0	1	0.122325	1.0000	nonperiodic-templates
0	1	0	1	1	1	2	0	2	2	0.739918	1.0000	nonperiodic-templates

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1	0	1	1	3	0	2	0	2	0	0.350485	1.0000	nonperiodic-templates
0	1	2.	0	1	0	2	3	0	1	0.350485	1.0000	nonperiodic-templates
0	0	1	3	0	1	2	2	1	0	0.350485	1.0000	nonperiodic-templates
0	1	0	1	2	3	1	1	1	0	0.534146	1.0000	nonperiodic-templates
4	0	2	1	1	0	1	0	0	1	0.122325	0.9000 *	nonperiodic-templates
1	1	1	1	0	1	2	1	1	1	0.991468	1.0000	nonperiodic-templates
0	2	1	0	2	1	1	1	1	1	0.911413	1.0000	nonperiodic-templates
0	0	0	0	1	0	3	2	2	2	0.213309	1.0000	nonperiodic-templates
1	0	1	1	0	0	3	0	2	2	0.350485	1.0000	nonperiodic-templates
2	1	0	2	0	0	2	0	1	2	0.534146	1.0000	nonperiodic-templates
3	1	1	0	3	1	0	1	0	0	0.213309	1.0000	nonperiodic-templates
2	2	1	1	1	1	1	0	1	0	0.911413	1.0000	nonperiodic-templates
2	1	3	0	0	1	0	0	2	1	0.350485	0.8000 *	nonperiodic-templates
3	1	1	0	2	1	1	0	1	0	0.534146	0.9000 *	nonperiodic-templates
2	2	1	0	1	1	0	1	1	1	0.911413	0.9000 *	nonperiodic-templates
4	1	2	0	1	1	0	0	1	0	0.122325	0.7000 *	nonperiodic-templates
3	3	1	0	0	0	1	1	1	0	0.213309	0.8000 *	nonperiodic-templates
5	1	0	0	1	0	1	1	1	0	0.017912	0.9000 *	nonperiodic-templates
0	0	0	2	3	1	1	2	0	1	0.350485	1.0000	nonperiodic-templates
0	1	1	0	2	4	1	0	0	1	0.122325	1.0000	nonperiodic-templates
0	1	2	0	2	2	0	3	0	0	0.213309	1.0000	nonperiodic-templates
0	1	1	0	2	0	2	0	4	0	0.066882	1.0000	nonperiodic-templates
1	1	1	1	2	0	3	1	0	0	0.534146	1.0000	nonperiodic-templates
1	1	0	1	1	2	1	1	1	1	0.991468	1.0000	nonperiodic-templates
3	1	2	1	1	0	0	0	2	0	0.350485	1.0000	apen
2	1	3	1	0	2	0	0	0	1	0.350485	1.0000	serial
0	2	1	2	2	1	1	0	0	1	0.739918	1.0000	serial

(10ns system clk $\frac{1}{2}$ cycle, 120 ps difference in frequency, 24 ps jitter zone sampled on the rising and falling edge for data sets 1 through q and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
6	1	1	1	0	0	1	0	0	0	0.000439	0.9000 *	frequency
3	2	1	1	1	1	1	0	0	0	0.534146	1.0000	block-frequency
6	0	2	1	0	0	0	0	1	0	0.000199	0.9000 *	cumulative-sums
7	0	1	1	0	1	0	0	0	0	0.000003		cumulative-sums
1	0	0	1	0	3	2	1	0	2	0.350485	1.0000	runs
1 1	0	1	1	2	1	1	1 2	1	1	0.991468 0.122325	0.9000 *	fft nonperiodic-templates
2	1	0	1	1	1	1	0	0	3	0.122323	1.0000 0.9000 *	nonperiodic-templates
1	2	0	2	2	1	1	1	0	0	0.739918	1.0000	nonperiodic-templates
2	0	0	2	0	1	1	1	1	2	0.739918	0.9000 *	nonperiodic-templates
2	0	2	0	0	0	1	3	1	1	0.350485	0.9000 *	nonperiodic-templates
1	1	0	1	0	3	2	1	0	1	0.534146	1.0000	nonperiodic-templates
0	3	1	1	0	2	1	0	2	0	0.350485	1.0000	nonperiodic-templates
0	1	1	0	0	0	1	3	2	2	0.350485	1.0000	nonperiodic-templates
0	1	1	3	0	1	1	2	1	0	0.534146	1.0000	nonperiodic-templates
1	0	2	2	0	2	1	1	1	0	0.739918	1.0000	nonperiodic-templates
1	1	1	0	3	1	1	1	1	0	0.739918	1.0000	nonperiodic-templates
0	2	0	1	0	0	1	2	3	1	0.350485	1.0000	nonperiodic-templates
1	1	0	1	1	1	2	2	1	0	0.911413	1.0000	nonperiodic-templates
2	0	0	2	1	1	0	2	2	0	0.534146	0.9000 *	nonperiodic-templates
1	3	1	1	0	3	0	0	0	1	0.213309	1.0000	nonperiodic-templates
1	1	0	0	2	0	2	1	1	2	0.739918	0.9000 *	nonperiodic-templates
1	0	0	2	0	2	2	2	1	0	0.534146	1.0000	nonperiodic-templates
0	0	0	1	1	1	1	2	1	3	0.534146	1.0000	nonperiodic-templates
0	1	2	2	1	1	0	1	2	0	0.739918	1.0000	nonperiodic-templates nonperiodic-templates
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1	2	1	1	1	0	1	2	0	1	0.122323	0.9000 *	nonperiodic-templates
1	0	0	2	2	1	1	0	1	2	0.739918	0.9000 *	nonperiodic-templates
0	0	1	1	2	2	0	1	3	0	0.350485	1.0000	nonperiodic-templates
1	0	1	0	0	2	1	3	0	2	0.350485	0.9000 *	nonperiodic-templates
1	0	0	2	0	3	2	1	1	0	0.350485	1.0000	nonperiodic-templates
1	1	0	0	2	2	1	1	0	2	0.739918	0.9000 *	nonperiodic-templates
1	2	0	3	0	1	1	1	0	1	0.534146	1.0000	nonperiodic-templates
3	1	0	2	0	1	1	1	0	1	0.534146	1.0000	nonperiodic-templates
1	1	0	2	1	2	2	0	1	0	0.739918	1.0000	nonperiodic-templates
3	1	1	0	0	0	1	1	2	1	0.534146	0.9000 *	nonperiodic-templates
2	1	1	2	3	0	0	0	1	0	0.350485	1.0000	nonperiodic-templates
2	1	2	0	0	1	1	2	0	1	0.739918	0.9000 *	nonperiodic-templates
1	3	0	1	2	1	1	0	1	0	0.534146	1.0000	nonperiodic-templates
3	1	0	0	0	1	1	1	2	1	0.534146	1.0000	nonperiodic-templates
1	1	0	0	3	2	1	1	1	0	0.534146	1.0000	nonperiodic-templates
2	1	2	0	0	1	0	0	2	2	0.534146	1.0000	nonperiodic-templates
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0	0	2	0	2	1	1	2	1	1	0.739918	1.0000	nonperiodic-templates
0	1	0	2	0	3	2	0	1	1	0.755510	1.0000	nonperiodic-templates
0	2	3	0	2	0	0	1	0	2	0.213309	1.0000	nonperiodic-templates
0	0	1	2	1	1	1	2	1	1	0.911413	1.0000	nonperiodic-templates
1	0	1	2	2	1	0	1	1	1	0.911413	1.0000	nonperiodic-templates
1	0	1	0	1	0	2	2	1	2	0.739918	1.0000	nonperiodic-templates
3	0	1	1	1	0	1	1	2	0	0.534146	0.7000 *	nonperiodic-templates
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1	0	0	1	1	1	3	1	1	1	0.739918	1.0000	nonperiodic-templates
0	1	1	0	3	1	1	0	2	1	0.534146	1.0000	nonperiodic-templates
2	1	1	3	2	0	0	1	0	0	0.350485	1.0000	nonperiodic-templates
1	1	2	1	1	0	1	1	1	1	0.991468	1.0000	nonperiodic-templates

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2.	0	0	2.	0	3	2.	0	0	1	0.213309	1.0000	nonperiodic-templates
1	0	0	0	0	2.	0	2	4	1	0.066882	1.0000	nonperiodic-templates
0	1	0	1	2.	1	2	0	0	3	0.350485	1.0000	nonperiodic-templates
4	0	2	1	1	1	0	1	0	0	0.122325	1.0000	nonperiodic-templates
1	0	1	0	0	1	3	0	3	1	0.213309	1.0000	nonperiodic-templates
1	0	2	0	0	2.	0	1	2.	2	0.534146	0.9000 *	nonperiodic-templates
1	0	2	0	2.	1	0	0	4	0	0.066882	1.0000	nonperiodic-templates
1	1	2	1	0	0	3	0	0	2	0.350485	1.0000	nonperiodic-templates
2	3	0	1	0	3	1	0	0	0	0.122325	1.0000	nonperiodic-templates
0	1	0	0	0	1	2.	1	4	1	0.122325	1.0000	nonperiodic-templates
1	0	4	0	0	0	1	2.	1	1	0.122325	1.0000	nonperiodic-templates
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3	0	0	0	_	0	•	2	1	2	0.213309	0.9000 *	nonperiodic-templates
3	1	2	2	0	0	1	0	0	1	0.350485	0.8000 *	nonperiodic-templates
0	2	0	1	3	1	1	1	0	1	0.534146	1.0000	nonperiodic-templates
1	1	0	1	0	2	0	1	3	1	0.534146	1.0000	nonperiodic-templates
0	0	5	0	0	1	0	1	1	2	0.008879	1.0000	nonperiodic-templates
1	0	0	1	0	1	1	2	4	0	0.122325	1.0000	nonperiodic-templates
2	1	2	0	1	1	0	1	1	1	0.911413	1.0000	nonperiodic-templates
0	1	1	1	0	2	3	1	0	1	0.534146	1.0000	nonperiodic-templates
1	1	1	0	1	0	1	1	3	1	0.739918	0.9000 *	nonperiodic-templates
0	1	0	1	1	1	0	2	3	1	0.534146	1.0000	nonperiodic-templates
0	0	1	1	1	2	2	1	1	1	0.911413	1.0000	nonperiodic-templates
0	2	3	0	2	0	1	1	0	1	0.350485	1.0000	apen
2	1	1	1	1	2	1	0	0	1	0.911413	1.0000	serial
1	1	1	2	1	0	3	1	0	0	0.534146	1.0000	serial

(10ns system clk $\frac{1}{2}$ cycle, 140 ps difference in frequency, 24 ps jitter zone sampled on the rising and falling edge for data sets a through f and consecutive outputs Xored)

			C4	 C5				C9	C10	P-VALUE	 P	 ROPORTIO)N	STATISTICAL TEST
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	frequency
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	block-frequency
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	cumulative-sums
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	cumulative-sums
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	runs
3	2	2	1	2	0	0	0	0	0	0.213309			*	fft
10	0	0	0	0	0	0	0	0	0	0.000000				nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000			*	nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000				nonperiodic-templates
9	0	0	0	1	0	0	0	0	0	0.000000				nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000				nonperiodic-templates
10	0	0	0	0	0		0	0	0	0.000000				nonperiodic-templates
8 2	0 2	2	0	0	0	0 1	0	0	0 1	0.000000 0.739918	^	0.9000		nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000	*			nonperiodic-templates nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000				nonperiodic-templates
9	0	1	0	0	0	0	0	0	0	0.000000				nonperiodic-templates
2	3	1	0	1	1	2	0	0	0	0.350485		0.9000		nonperiodic-templates
8	1	0	0	0	0	1	0	0	0	0.000000	*			nonperiodic-templates
4	1	1	1	1	0	1	1	0	0	0.213309		0.8000		nonperiodic-templates
6	1	1	0	0	0	0	0	2	0	0.000199		0.8000		nonperiodic-templates
1	0	1	2	1	1	1	1	0	2	0.911413		0.9000		nonperiodic-templates
8	0	0	1	0	0	0	1	0	0	0.000000	*	0.5000	*	nonperiodic-templates
6	1	1	1	1	0	0	0	0	0	0.000439		0.8000	*	nonperiodic-templates
1	2	2	1	0	1	1	0	2	0	0.739918		1.0000		nonperiodic-templates
9	1	0	0	0	0	0	0	0	0	0.000000	*	0.6000	*	nonperiodic-templates
5	0	2	0	0	0	0	2	0	1	0.004301		0.7000		nonperiodic-templates
3	1	1	2	1	1	1	0	0	0	0.534146		0.9000	*	nonperiodic-templates
1	0	0	2	1	3	0	2	0	1	0.350485		1.0000		nonperiodic-templates
6	1	1	1	1	0	0	0	0	0	0.000439		0.7000		nonperiodic-templates
5	1	0	0	0	0	0	2	0	2	0.004301			*	nonperiodic-templates
2	0	0 3	0	1	1	2	0	3	1	0.350485		0.9000	*	nonperiodic-templates
0 2	1 2	1	0	0	1	0	0	1	0	0.035174		1.0000		nonperiodic-templates
2	1	0	0	0	1	1	3	2	0	0.350485		1.0000	*	nonperiodic-templates nonperiodic-templates
0	0	1	0	0	1	3	1	3	1	0.213309		1.0000		nonperiodic-templates
1	1	0	0	1	1	2	2	2	0	0.739918		1.0000		nonperiodic-templates
8	0	0	1	1	0	0	0	0	0	0.000000	*		*	nonperiodic-templates
7	1	0	0	0	0	1	1	0	0	0.000003	*		*	nonperiodic-templates
1	2	2	0	1	1	2	0	1	0	0.739918		1.0000		nonperiodic-templates
7	0	0	1	0	2	0	0	0	0	0.000001	*		*	nonperiodic-templates
3	2	1	0	0	0	1	0	1	2	0.350485		0.8000	*	nonperiodic-templates
1	0	2	0	0	4	1	1	1	0	0.122325		1.0000		nonperiodic-templates
0	3	1	0	0	0	1	3	1	1	0.213309		1.0000		nonperiodic-templates
1	1	1	2	1	2	1	0	1	0	0.911413		1.0000		nonperiodic-templates
1	1	3	0	2	1	1	0	1	0	0.534146		1.0000		nonperiodic-templates
2	0	1	0	1	1	3	0	1	1	0.534146		1.0000		nonperiodic-templates
3	2	2	0	1	1	0	0	1	0	0.350485		1.0000		nonperiodic-templates
0	0	0	2	1	2	0	3	1	1	0.350485		1.0000		nonperiodic-templates
2	0	0	1	0	2	2	0	2	1	0.534146		0.9000	*	nonperiodic-templates
0	1	1	1	0	1	1	0	4	1	0.213309		1.0000		nonperiodic-templates
2	1	0	0	1	1	0	1	3	1	0.534146		1.0000		nonperiodic-templates
1	2	1	0	0	1	2	1 2	1	1	0.911413		1.0000	*	nonperiodic-templates
4 0	0	0	2 1	0	4	3	1	0	1	0.066882		0.8000	^	nonperiodic-templates nonperiodic-templates
0	2	2	2	2	1	0	1	0	0	0.035174 0.534146		1.0000		nonperiodic-templates nonperiodic-templates
0	1	1	0	4	3	1	0	0	0	0.035174		1.0000		nonperiodic-templates nonperiodic-templates
U	T	Т	U	4	3	Т	U	U	U	0.0331/4		1.0000		momper rourc-remprates

0	0	0	1	0	2	4	0	2	1	0.066882		1.0000		nonperiodic-templates
0	1 1	1 1	0 1	0 2	2	0 1	3 1	3 1	0 1	0.122325 0.991468		1.0000		nonperiodic-templates nonperiodic-templates
0	0	1	1	3	2	1	1	1	0	0.534146		1.0000		nonperiodic-templates
0	2	1	1	1	2	3	0	0	0	0.350485		1.0000		nonperiodic-templates
1	0	0	0	3	2	1	0	1	2	0.350485		1.0000		nonperiodic-templates
0 9	0	0	3 0	2	0	0	3 0	1 1	1	0.122325	k-	1.0000	*	nonperiodic-templates
5	0 1	1	0	1	0	1	0	0	1	0.0000000 * 0.017912		0.7000		nonperiodic-templates nonperiodic-templates
2	1	0	2	1	1	1	2	0	0	0.739918		1.0000		nonperiodic-templates
4	0	0	1	2	0	0	0	1	2	0.066882		1.0000		nonperiodic-templates
6	1	1	0	0	0	1	0	1	0	0.000439		0.8000	*	nonperiodic-templates
0 1	1 3	1	2	2 1	1	2 1	0 2	0	1	0.739918 0.350485		1.0000		nonperiodic-templates nonperiodic-templates
3	1	1	0	1	3	0	0	1	0	0.213309		0.8000	*	nonperiodic-templates
0	0	4	0	1	1	1	0	2	1	0.122325		1.0000		nonperiodic-templates
1	0	1	2	2	2	0	2	0	0	0.534146		1.0000		nonperiodic-templates
0	0	2 1	1 1	1 3	1 2	1	1 0	1 2	2	0.911413 0.350485		1.0000		nonperiodic-templates
3	2	2	1	0	1	0	0	0	1	0.350485		0.9000	*	nonperiodic-templates nonperiodic-templates
0	1	2	0	2	1	1	0	1	2	0.739918		1.0000		nonperiodic-templates
0	0	3	1	1	2	0	0	3	0	0.122325		1.0000		nonperiodic-templates
2	0	1	1	0	1	2	1	2	0	0.739918		1.0000		nonperiodic-templates
0 1	1	0 3	3 0	1	1 1	1	2 1	0 2	1 1	0.534146 0.534146		1.0000		nonperiodic-templates nonperiodic-templates
1	0	1	0	3	1	2	0	2	0	0.350485		1.0000		nonperiodic-templates
0	1	2	1	1	0	3	0	1	1	0.534146		1.0000		nonperiodic-templates
0	2	1	1	1	1	3	0	1	0	0.534146		1.0000		nonperiodic-templates
0	1	1	2	1	3	0	0	2	0	0.350485		1.0000		nonperiodic-templates
0 5	0	0 1	4 1	3 0	1	2	0 1	0	0	0.017912 0.008879		1.0000	*	nonperiodic-templates nonperiodic-templates
0	0	0	2	0	0	5	1	2	0	0.004301		1.0000		nonperiodic-templates
2	1	1	1	0	0	0	3	1	1	0.534146		1.0000		nonperiodic-templates
1	0	1	0	1	1	2	2	1	1	0.911413		0.9000	*	nonperiodic-templates
0	0	2	1	4	2	1	0	0	0	0.066882		1.0000		nonperiodic-templates
0 1	1 2	0	0 2	2	0	3 1	2 2	1 1	1 1	0.350485 0.739918		1.0000		nonperiodic-templates nonperiodic-templates
0	1	0	2	2	1	2	1	0	1	0.739918		1.0000		nonperiodic-templates
0	0	1	1	1	3	0	0	3	1	0.213309		1.0000		nonperiodic-templates
1	2	3	0	2	1	1	0	0	0	0.350485		1.0000		nonperiodic-templates
0 1	2	2 1	0 1	0 1	1 4	3 0	1 0	0	1 2	0.350485 0.122325		1.0000		nonperiodic-templates nonperiodic-templates
0	2	2	0	2	0	1	0	2	1	0.122323		1.0000		nonperiodic-templates
1	1	1	0	1	4	1	1	0	0	0.213309		1.0000		nonperiodic-templates
1	1	1	1	2	1	1	1	1	0	0.991468		1.0000		nonperiodic-templates
0	1	3	2	1	0	1	0	2	0	0.350485		1.0000		nonperiodic-templates
0 3	1 2	3 0	1 2	0 1	1	2	1	1 1	0	0.534146 0.350485		1.0000		nonperiodic-templates nonperiodic-templates
0	0	5	1	1	1	2	0	0	0	0.008879		1.0000		nonperiodic-templates
8	1	0	0	1	0	0	0	0	0	0.0000000 *	k	0.5000	*	nonperiodic-templates
3	0	1	0	0	2	0	2	2	0	0.213309		1.0000		nonperiodic-templates
3 0	0	0	2	3 0	0 1	0 3	1	1 3	0 2	0.122325		0.9000	*	nonperiodic-templates nonperiodic-templates
3	2	0	1	1	0	2	1	0	0	0.122325 0.350485		0.9000	*	nonperiodic-templates
0	1	0	1	1	0	2	2	1	2	0.739918		1.0000		nonperiodic-templates
2	2	1	0	2	1	0	1	0	1	0.739918		1.0000		nonperiodic-templates
1	1	1	0	2	1	2	0	1	1	0.911413		1.0000	al.	nonperiodic-templates
3 0	0 1	0 1	1 2	0 1	0	1	4 3	1	0 2	0.035174 0.350485		0.9000	*	nonperiodic-templates nonperiodic-templates
1	0	0	2	0	1	2	2	0	2	0.534146		1.0000		nonperiodic-templates
0	0	3	2	0	2	0	1	1	1	0.350485		1.0000		nonperiodic-templates
1	1	0	2	0	1	1	1	2	1	0.911413		1.0000		nonperiodic-templates
1	1	3	1	0	2	0	0	1	1	0.534146		1.0000		nonperiodic-templates
0	1	1 2	0 1	1 1	2	2 1	1 0	0	2	0.739918 0.350485		1.0000		nonperiodic-templates nonperiodic-templates
3	1	1	0	3	1	0	1	0	0	0.213309		0.8000	*	nonperiodic-templates
0	1	1	1	0	5	0	0	1	1	0.017912		1.0000		nonperiodic-templates
0	1	0	0	1	1	2	2	2	1	0.739918		1.0000		nonperiodic-templates
0	0	2	3	2	3	2	0	1	0	0.213309		1.0000	*	nonperiodic-templates
1	1	0 3	3 1	2	2	1	0	0 1	0	0.350485 0.350485		0.9000		nonperiodic-templates nonperiodic-templates
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0	1	0	2	3	0	0	1	3	0	0.122325		1.0000		nonperiodic-templates
0	2	1	1	1	3	2	0	0	0	0.350485		1.0000		nonperiodic-templates
0	1	2	2	0	1	0	3	1	0	0.350485		1.0000		nonperiodic-templates
0	1	4	0	0	1	0	2	2	0	0.066882		1.0000		nonperiodic-templates
1	3	3	1	1	1	0	0	0	0	0.213309		1.0000		nonperiodic-templates
0	0	0	2	1	2	1	1	1	2	0.739918		1.0000		nonperiodic-templates
1	1	3	0	1	0	1	1	2	0	0.534146		1.0000		nonperiodic-templates
1	1	3	1	2	1	0	1	0	0	0.534146		1.0000		nonperiodic-templates
2	1	2	0	1	2	1	0	1	0	0.739918		1.0000		nonperiodic-templates
2	0	1	0	3	1	1	0	1	1	0.534146		1.0000		nonperiodic-templates
0	0	1	1	2	4	2	0	0	0	0.066882		1.0000		nonperiodic-templates
0	0	1	0	3	1	2	0	1	2	0.350485		1.0000		nonperiodic-templates
1	0	1	4	2	1	0	0	0	1	0.122325		1.0000		nonperiodic-templates
0	0	3	1	1	0	2	1	1	1	0.534146		1.0000		nonperiodic-templates
1	2	0	1	0	3	3	0	0	0	0.122325		1.0000		nonperiodic-templates
2	2	1	1	2	1	1	0	0	0	0.739918		1.0000		nonperiodic-templates
2	5	3	0	0	0	0	0	0	0	0.000954		1.0000		nonperiodic-templates
0	3	0	2	2	1	1	0	0	1	0.350485		1.0000		nonperiodic-templates
0	4	2	2	1	0	1	0	0	0	0.066882		1.0000		nonperiodic-templates
4	1	2	3	0	0	0	0	0	0	0.017912		1.0000		nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	nonperiodic-templates
6	0	0	1	3	0	0	0	0	0	0.000040	*	0.6000	*	nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	nonperiodic-templates
6	1	1	1	1	0	0	0	0	0	0.000439		0.8000	*	nonperiodic-templates
7	2	0	1	0	0	0	0	0	0	0.000001	*	0.5000	*	nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	apen
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	serial
5	1	1	1	1	1	0	0	0	0	0.017912		0.9000	*	serial

For further guidelines construct a probability table using the MAPLE program provided in the addendum section of the documentation.

(10ns system clk $\frac{1}{2}$ cycle, 140 ps difference in frequency, 24 ps jitter zone sampled on the rising and falling edge for data sets 1 through q and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
6	1	1	1	0	0	1	0	0	0	0.000439	0.9000 *	frequency
3	2	1	1	1	1	1	0	0	0	0.534146	1.0000	block-frequency
6	0	2	1	0	0	0	0	1	0	0.000199	0.9000 *	cumulative-sums
7	0	1	1	0	1	0	0	0	0	0.000003	* 0.8000 *	cumulative-sums
1	0	0	1	0	3	2	1	0	2	0.350485	1.0000	runs
1	0	1	1	2	1	1	1	1	1	0.991468	0.9000 *	fft
1	0	0	1	0	1	1	2	4	0	0.122325	1.0000	nonperiodic-templates
2	1	0	1	1	1	1	0	0	3	0.534146	0.9000 *	nonperiodic-templates
1	2	0	2	2	1	1	1	0	0	0.739918	1.0000	nonperiodic-templates
2	0	0	2	0	1	1	1	1	2	0.739918	0.9000 *	nonperiodic-templates
2	0	2	0	0	0	1	3	1	1	0.350485	0.9000 *	nonperiodic-templates
1	1	0	1	0	3	2	1	0	1	0.534146	1.0000	nonperiodic-templates
0	3	1	1	0	2	1	0	2	0	0.350485	1.0000	nonperiodic-templates
0	1	1	0	0	0	1	3	2	2	0.350485	1.0000	nonperiodic-templates
0	1	1	3	0	1	1	2	1	0	0.534146	1.0000	nonperiodic-templates
1	0	2	2	0	2	1	1	1	0	0.739918	1.0000	nonperiodic-templates
1	1 2	0	1	3	0	1	2	3	0 1	0.739918 0.350485	1.0000	nonperiodic-templates
1	1	0	1	1	1	2	2	1	0	0.911413	1.0000 1.0000	nonperiodic-templates nonperiodic-templates
2	0	0	2	1	1	0	2	2	0	0.534146	0.9000 *	nonperiodic-templates
1	3	1	1	0	3	0	0	0	1	0.213309	1.0000	nonperiodic-templates
1	1	0	0	2	0	2	1	1	2	0.739918	0.9000 *	nonperiodic-templates
1	0	0	2	0	2	2	2	1	0	0.534146	1.0000	nonperiodic-templates
0	0	0	1	1	1	1	2	1	3	0.534146	1.0000	nonperiodic-templates
0	1	2	2	1	1	0	1	2	0	0.739918	1.0000	nonperiodic-templates
0	0	1	3	1	0	3	1	0	1	0.213309	1.0000	nonperiodic-templates
1	0	0	0	1	2	1	1	4	0	0.122325	1.0000	nonperiodic-templates
1	2	1	1	1	0	1	2	0	1	0.911413	0.9000 *	nonperiodic-templates
1	0	0	2	2	1	1	0	1	2	0.739918	0.9000 *	nonperiodic-templates
0	0	1	1	2	2	0	1	3	0	0.350485	1.0000	nonperiodic-templates
1	0	1	0	0	2	1	3	0	2	0.350485	0.9000 *	nonperiodic-templates
1	0	0	2	0	3	2	1	1	0	0.350485	1.0000	nonperiodic-templates
1	1	0	0	2	2	1	1	0	2	0.739918	0.9000 *	nonperiodic-templates
1	2	0	3	0	1	1	1	0	1	0.534146	1.0000	nonperiodic-templates
3	1	0	2	0	1	1	1	0	1	0.534146	1.0000	nonperiodic-templates
1	1	0	2	1	2	2	0	1	0	0.739918	1.0000	nonperiodic-templates
3	1	1	0	0	0	1	1	2	1	0.534146	0.9000 *	nonperiodic-templates
2	1	1 2	2	3	0	0	0	1	0	0.350485	1.0000	nonperiodic-templates
2	1	0	0 1	0 2	1	1	2	0	1	0.739918 0.534146	0.9000 * 1.0000	nonperiodic-templates nonperiodic-templates
3	1	0	0	0	1	1	1	2	1	0.534146	1.0000	nonperiodic-templates
1	1	0	0	3	2	1	1	1	0	0.534146	1.0000	nonperiodic-templates
2	1	2	0	0	1	0	0	2	2	0.534146	1.0000	nonperiodic-templates
0	1	1	0	0	0	4	0	2	2	0.066882	1.0000	nonperiodic-templates
0	0	1	1	3	0	2	1	1	1	0.534146	1.0000	nonperiodic-templates
3	1	0	0	1	1	1	2	1	0	0.534146	1.0000	nonperiodic-templates
0	0	2	0	2	1	1	2	1	1	0.739918	1.0000	nonperiodic-templates
0	1	0	2	0	3	2	0	1	1	0.350485	1.0000	nonperiodic-templates
0	2	3	0	2	0	0	1	0	2	0.213309	1.0000	nonperiodic-templates
0	0	1	2	1	1	1	2	1	1	0.911413	1.0000	nonperiodic-templates
1	0	1	2	2	1	0	1	1	1	0.911413	1.0000	nonperiodic-templates
1	0	1	0	1	0	2	2	1	2	0.739918	1.0000	nonperiodic-templates
3	0	1	1	1	0	1	1	2	0	0.534146	0.7000 *	nonperiodic-templates
0	0	1	1	2	1	0	0	2	3	0.350485	1.0000	nonperiodic-templates
1	0	0	1	1	1	3	1	1	1	0.739918	1.0000	nonperiodic-templates
0	1	1	0	3	1	1	0	2	1	0.534146	1.0000	nonperiodic-templates
2	1	1	3	2	0	0	1	0	0	0.350485	1.0000	nonperiodic-templates
1	1	2	1	1	0	1	1	1	1	0.991468	1.0000	nonperiodic-templates

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2.	0	0	2.	0	3	2.	0	0	1	0.213309	1.0000	nonperiodic-templates
1	0	0	0	0	2.	0	2	4	1	0.066882	1.0000	nonperiodic-templates
0	1	0	1	2.	1	2	0	0	3	0.350485	1.0000	nonperiodic-templates
4	0	2	1	1	1	0	1	0	0	0.122325	1.0000	nonperiodic-templates
1	0	1	0	0	1	3	0	3	1	0.213309	1.0000	nonperiodic-templates
1	0	2	0	0	2.	0	1	2.	2	0.534146	0.9000 *	nonperiodic-templates
1	0	2	0	2.	1	0	0	4	0	0.066882	1.0000	nonperiodic-templates
1	1	2	1	0	0	3	0	0	2	0.350485	1.0000	nonperiodic-templates
2	3	0	1	0	3	1	0	0	0	0.122325	1.0000	nonperiodic-templates
0	1	0	0	0	1	2.	1	4	1	0.122325	1.0000	nonperiodic-templates
1	0	4	0	0	0	1	2.	1	1	0.122325	1.0000	nonperiodic-templates
0	0	0	0	0	3	4	1	0	2.	0.122323	1.0000	nonperiodic-templates
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3	0	0	0	_	0	•	2	1	2	0.213309	0.9000 *	nonperiodic-templates
3	1	2	2	0	0	1	0	0	1	0.350485	0.8000 *	nonperiodic-templates
0	2	0	1	3	1	1	1	0	1	0.534146	1.0000	nonperiodic-templates
1	1	0	1	0	2	0	1	3	1	0.534146	1.0000	nonperiodic-templates
0	0	5	0	0	1	0	1	1	2	0.008879	1.0000	nonperiodic-templates
1	0	0	1	0	1	1	2	4	0	0.122325	1.0000	nonperiodic-templates
2	1	2	0	1	1	0	1	1	1	0.911413	1.0000	nonperiodic-templates
0	1	1	1	0	2	3	1	0	1	0.534146	1.0000	nonperiodic-templates
1	1	1	0	1	0	1	1	3	1	0.739918	0.9000 *	nonperiodic-templates
0	1	0	1	1	1	0	2	3	1	0.534146	1.0000	nonperiodic-templates
0	0	1	1	1	2	2	1	1	1	0.911413	1.0000	nonperiodic-templates
0	2	3	0	2	0	1	1	0	1	0.350485	1.0000	apen
2	1	1	1	1	2	1	0	0	1	0.911413	1.0000	serial
1	1	1	2	1	0	3	1	0	0	0.534146	1.0000	serial

(10ns system clk $\frac{1}{2}$ cycle, 160 ps difference in frequency, 24 ps jitter zone sampled on the rising and falling edge for data sets a through f and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.0000 *	frequency
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.0000 *	block-frequency
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.0000 *	cumulative-sums
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.0000 *	cumulative-sums
10	0	0	0	0	0	0	0	0	0	0.000000	* 0.0000 *	runs
2	3	0	0	0	1	3	0	0	1	0.122325	0.9000 *	fft
8	1	0	0	0	0	0	1	0	0	0.000000	* 0.4000 *	nonperiodic-templates
5	0	1	3	0	0	0	0	0	1	0.002043	0.6000 *	nonperiodic-templates
6	1	0	1	0	0	0	0	1	1	0.000439	0.7000 *	nonperiodic-templates
2	1	2	0	0	2	1	1	1	0	0.739918	0.9000 *	nonperiodic-templates
5	3	1	1	0	0	0	0	0	0	0.002043	0.9000 *	nonperiodic-templates
1	2	2	0	0	0	2	2	1	0	0.534146	0.9000 *	nonperiodic-templates
2	1	1	0	2	1	2	0	0	1	0.739918	0.9000 *	nonperiodic-templates
1	0	0	1	1	0	1	1	3	2	0.534146	1.0000	nonperiodic-templates
6	0	1	0	1	2	0	0	0	0	0.000199	0.7000 *	nonperiodic-templates
0	2	2	1	1	0	1	1	0	2	0.739918	1.0000	nonperiodic-templates
3	1	0	1	0	0	1	2	1	1	0.534146	0.8000 *	nonperiodic-templates
1 2	0	3	2	3	1	2	1	2	1	0.350485	1.0000	nonperiodic-templates nonperiodic-templates
0	3	0	0	0	1	1	3	1	1	0.350485	0.9000 *	• •
1	1	3	1	0	2	0	1	0	1	0.213309 0.534146	1.0000 0.9000 *	nonperiodic-templates nonperiodic-templates
0	0	0	0	0	3	2	1	3	1	0.122325	1.0000	nonperiodic-templates
0	3	1	0	0	1	0	3	2	0	0.122325	1.0000	nonperiodic-templates
1	3	1	1	2	1	0	0	0	1	0.534146	1.0000	nonperiodic-templates
0	2	1	0	0	0	2	2	1	2	0.534146	1.0000	nonperiodic-templates
3	0	1	0	2	2	0	1	1	0	0.350485	0.8000 *	nonperiodic-templates
2	0	1	3	0	0	1	1	1	1	0.534146	1.0000	nonperiodic-templates
1	2	1	3	1	1	1	0	0	0	0.534146	0.9000 *	nonperiodic-templates
1	0	0	2	0	3	1	0	2	1	0.350485	1.0000	nonperiodic-templates
2	1	1	0	1	0	1	1	3	0	0.534146	1.0000	nonperiodic-templates
3	1	0	1	1	0	1	0	2	1	0.534146	1.0000	nonperiodic-templates
3	1	2	1	0	0	1	0	1	1	0.534146	0.9000 *	nonperiodic-templates
1	1	0	1	0	0	3	0	1	3	0.213309	1.0000	nonperiodic-templates
1	0	0	1	0	1	1	4	0	2	0.122325	1.0000	nonperiodic-templates
0	1	1	0	3	2	1	1	1	0	0.534146	1.0000	nonperiodic-templates
0	0	1	0	1	2	1	1	1	3	0.534146	1.0000	nonperiodic-templates
2	0	1	0	1	1	1	0	4	0	0.122325	0.9000 *	nonperiodic-templates
3	1	0	2	1	0	1	0	1	1	0.534146	1.0000	nonperiodic-templates
3	2	0	1	0	0	1	0	3	0	0.122325	0.7000 *	nonperiodic-templates
1	1	0	2	1	1	1	1	1	1	0.991468	1.0000	nonperiodic-templates
4	2	0	0	2	0	1	0	1	0	0.066882	0.9000 *	nonperiodic-templates
2	1	0	0	0	2	1	2	1	1	0.739918	0.9000 *	nonperiodic-templates
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0	1	0	2	1	0	0	3	1	2	0.122323	1.0000	nonperiodic-templates
0	1	2	1	0	0	2	2	1	1	0.739918	1.0000	nonperiodic-templates
0	1	2	2	0	2	0	1	1	1	0.739918	1.0000	nonperiodic-templates
4	0	2	0	0	1	0	1	2	0	0.066882	1.0000	nonperiodic-templates
0	2	3	1	2	1	1	0	0	0	0.350485	1.0000	nonperiodic-templates
5	2	0	2	0	0	1	0	0	0	0.004301	0.9000 *	nonperiodic-templates
1	2	1	1	0	2	2	1	0	0	0.739918	0.9000 *	nonperiodic-templates
0	0	1	2	2	0	1	3	1	0	0.350485	1.0000	nonperiodic-templates
1	0	0	0	2	2	0	0	2	3	0.213309	1.0000	nonperiodic-templates
0	1	0	1	1	1	1	1	1	3	0.739918	1.0000	nonperiodic-templates

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0	0	0	2	2	3	0	1	1	1	0.350485		1.0000		nonperiodic-templates
0	2	1	1	0	0	1	3	2	0	0.350485		1.0000		nonperiodic-templates
0	1	2	1	2	1	0	3	0	0	0.350485		1.0000		nonperiodic-templates
1	0	0	0	0	1	2	0	6	0	0.000199		1.0000		nonperiodic-templates
0	2	1	3	0	1	3	0	0	0	0.122325		1.0000		nonperiodic-templates
0	1	2	0	3	2	0	0	1	1	0.350485		1.0000		nonperiodic-templates
1	0	1	1	1	2	2	0	1	1	0.911413		1.0000		nonperiodic-templates
1	0	1	1	1	1	1	2	1	1	0.991468		1.0000		nonperiodic-templates
3	0	0	1	1	0	2	0	2	1	0.350485		1.0000		nonperiodic-templates
1	1	1	0	1	0	2	1	1	2	0.911413		0.9000	*	nonperiodic-templates
3	1	1	1	1	0	0	3	0	0	0.213309		1.0000		nonperiodic-templates
0	1	0	2	1	1	2	2	1	0	0.739918		1.0000		nonperiodic-templates
1	1	1	0	3	0	2	1	0	1	0.534146		1.0000		nonperiodic-templates
0	1	0	0	1	1	1	1	3	2	0.534146		1.0000		nonperiodic-templates
0	1	2	1	1	2	0	1	1	1	0.911413		1.0000		nonperiodic-templates
0	1	1	3	2	2	0	0	1	0	0.350485		1.0000		nonperiodic-templates
0	1	1	1	2	1	1	2	1	0	0.911413		1.0000		nonperiodic-templates
1	2	2	0	2	2	0	1	0	0	0.534146		1.0000		nonperiodic-templates
0	0	0	2	4	1	0	1	2	0	0.066882		1.0000		nonperiodic-templates
8	1	0	0	0	0	0	1	0	0	0.000000	*	0.4000	*	nonperiodic-templates
6	2	0	1	0	1	0	0	0	0	0.000199		0.6000	*	nonperiodic-templates
1	1	2	1	0	0	0	1	1	3	0.534146		1.0000		nonperiodic-templates
6	1	1	1	1	0	0	0	0	0	0.000439		0.7000	*	nonperiodic-templates
3	3	3	0	0	1	0	0	0	0	0.035174		0.9000	*	nonperiodic-templates
5	0	0	1	0	1	1	2	0	0	0.008879		0.8000	*	nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	apen
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.1000	*	serial
0	1	1	0	1	0	3	2	0	2	0.350485		1.0000		serial

(10ns system clk $\frac{1}{2}$ cycle, 160 ps difference in frequency, 24 ps jitter zone sampled on the rising and falling edge for data sets 1 through q and consecutive outputs Xored)

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
10	0	0	0	0	0	0	0	0	0		* 0.0000 *	frequency
10	0	0	0	0	0	0	0	0	0		* 0.0000 *	block-frequency
10	0	0	0	0	0	0	0	0	0		* 0.0000 *	cumulative-sums
10	0	0	0	0	0	0	0	0	0		* 0.0000 *	cumulative-sums
10	0	0	0	0	0	0	0	0	0		* 0.0000 *	runs
3	1	1	1	1	2	0	1	0	0	0.534146	0.9000 *	fft
8	0	2	0	0	0	0	0	0	0		* 0.9000 *	nonperiodic-templates
2	2	1	1	1	0	1	1	1	0	0.911413	1.0000	nonperiodic-templates
6	1	0	3	0	0	0	0	0	0		* 0.7000 *	nonperiodic-templates
1	2	2	0	1	1	1	1	1	0	0.911413	1.0000	nonperiodic-templates
4	1	1	1	0	1	0	1	0	1	0.213309	0.9000 *	nonperiodic-templates
3	0	1	1	2	0	2	1	0	0	0.350485	0.9000 *	nonperiodic-templates
4	0	1	0	1	2	0	0	2	0	0.066882	0.7000 *	nonperiodic-templates
3	0	2	1	1	0	1	0	2	0	0.350485	0.9000 *	nonperiodic-templates
6	2	0	0	1	0	0	1	0	0	0.000199	0.7000 *	nonperiodic-templates
2	2	0	2	0	0	0	2	0	2	0.350485	0.9000 *	nonperiodic-templates
4	2	0	1 2	2	0	0	1	0	0 2	0.066882	0.8000 *	nonperiodic-templates
3	3	2	0	0	0	1	1	0	0	0.122325	1.0000	nonperiodic-templates
2	1	2	0	0	1	1	1	1	1	0.122323	1.0000	nonperiodic-templates nonperiodic-templates
3	0	1	1	0	1	0	2	1	1	0.534146	1.0000	nonperiodic-templates
1	1	1	0	3	0	1	0	1	2	0.534146	1.0000	nonperiodic-templates
1	2	0	2	0	0	2	1	0	2	0.534146	1.0000	nonperiodic-templates
3	1	1	0	0	1	3	1	0	0	0.213309	0.9000 *	nonperiodic-templates
1	1	0	2	2	2	0	0	0	2	0.534146	1.0000	nonperiodic-templates
4	0	1	1	2	1	0	0	1	0	0.122325	0.9000 *	nonperiodic-templates
3	2	2	1	1	0	0	1	0	0	0.350485	0.9000 *	nonperiodic-templates
0	1	0	0	0	3	1	1	4	0	0.035174	1.0000	nonperiodic-templates
0	0	2	0	3	2	1	1	1	0	0.350485	1.0000	nonperiodic-templates
1	2	2	0	0	0	2	2	1	0	0.534146	1.0000	nonperiodic-templates
4	0	1	0	1	2	0	1	0	1	0.122325	0.9000 *	nonperiodic-templates
2	0	2	0	2	2	0	1	1	0	0.534146	1.0000	nonperiodic-templates
1	1	1	1	1	0	1	1	2	1	0.991468	1.0000	nonperiodic-templates
3	3	2	0	0	0	0	1	0	1	0.122325	1.0000	nonperiodic-templates
1	1	0	1	2	1	1	1	1	1	0.991468	1.0000	nonperiodic-templates
1	0	0	1	2	1	3	1	1	0	0.534146	1.0000	nonperiodic-templates
0	1	0	0	4	2	1	0	1	1	0.122325	1.0000	nonperiodic-templates
5	2	0	0	0	0	2	1	0	0	0.004301	0.8000 *	nonperiodic-templates
3	2	0	0	0	2	1	1	1	0	0.350485	0.9000 *	nonperiodic-templates
1	2	0	2	1	0	1	2	1	0	0.739918	1.0000	nonperiodic-templates
6	1	0	1	1	1	0	0	0	0	0.000439	0.8000 *	nonperiodic-templates
0	1	3	1	2	1	0	1	1	0	0.534146	1.0000	nonperiodic-templates
1	0	1	0	1	2	2	3	0	0	0.350485	1.0000	nonperiodic-templates
3	1	1	0	2	0	1	1	1	0	0.534146	1.0000	nonperiodic-templates
0	1	2	1	1	1	0	1	1	2	0.911413	1.0000	nonperiodic-templates
3	0	1	0	0	1	2	2	0	1	0.350485	0.9000 *	nonperiodic-templates
1	1	1	0	0	2	2	1	0	2	0.739918	0.9000 *	nonperiodic-templates
2	1	0	1	1	2	0	1	2	0	0.739918	0.9000 *	nonperiodic-templates
0	1	0	1	1	1	0	4	1	1	0.213309	1.0000	nonperiodic-templates
2	0	1	0	3	0	1	0	3	0	0.122325	0.9000 *	nonperiodic-templates
0	2	2	1	0	0	4	1	0	0	0.066882	1.0000	nonperiodic-templates
3	0	0	0	1	0	0	0	1	3	0.213309	0.9000 *	nonperiodic-templates
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0	0	1	3	2	0	1	1	0	2	0.739918	0.9000 *	nonperiodic-templates nonperiodic-templates
1	1	0	0	1	2	0	1	3	1	0.534146	1.0000 0.9000 *	nonperiodic-templates
1	0	1	1	3	1	1	0	2	0	0.534146	1.0000	nonperiodic-templates
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                                             0.350485
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                                                                     nonperiodic-templates
```

0	4	1	0	2	0	0	1	2	0	0.066882		1.0000		nonperiodic-templates
0	1	1	1	0	2	0	2	3	0	0.350485		1.0000		nonperiodic-templates
1	0	0	0	3	0	1	0	3	2	0.122325		1.0000		nonperiodic-templates
1	1	1	0	2	0	4	1	0	0	0.122325		1.0000		nonperiodic-templates
0	1	0	1	2	1	1	3	1	0	0.534146		1.0000		nonperiodic-templates
0	1	1	0	0	1	3	1	2	1	0.534146		1.0000		nonperiodic-templates
1	0	2	2	0	0	0	2	1	2	0.534146		1.0000		nonperiodic-templates
0	2	0	2	0	4	1	0	1	0	0.066882		1.0000		nonperiodic-templates
0	0	0	1	1	0	6	2	0	0	0.000199		1.0000		nonperiodic-templates
1	0	3	1	2	0	0	1	1	1	0.534146		1.0000		nonperiodic-templates
0	0	0	0	2	1	0	1	2	4	0.066882		1.0000		nonperiodic-templates
0	1	0	2	1	1	2	2	1	0	0.739918		1.0000		nonperiodic-templates
0	0	1	1	1	0	1	3	2	1	0.534146		1.0000		nonperiodic-templates
0	0	0	2	1	1	2	2	1	1	0.739918		1.0000		nonperiodic-templates
0	0	1	2	2	1	1	1	2	0	0.739918		1.0000		nonperiodic-templates
0	1	1	1	3	0	1	2	1	0	0.534146		1.0000		nonperiodic-templates
0	0	3	2	2	1	0	1	0	1	0.350485		1.0000		nonperiodic-templates
0	4	0	3	1	0	1	0	1	0	0.035174		1.0000		nonperiodic-templates
0	3	1	1	1	1	0	1	0	2	0.534146		1.0000		nonperiodic-templates
1	0	2	2	2	1	1	1	0	0	0.739918		1.0000		nonperiodic-templates
8	0	2	0	0	0	0	0	0	0	0.000000	*	0.9000	*	nonperiodic-templates
7	1	0	1	1	0	0	0	0	0	0.000003	*	0.6000	*	nonperiodic-templates
1	1	1	2	1	0	2	2	0	0	0.739918		1.0000		nonperiodic-templates
5	1	0	1	1	2	0	0	0	0	0.008879		0.7000	*	nonperiodic-templates
2	3	3	2	0	0	0	0	0	0	0.066882		1.0000		nonperiodic-templates
3	1	2	0	1	0	2	0	1	0	0.350485		1.0000		nonperiodic-templates
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.0000	*	apen
10	0	0	0	0	0	0	0	0	0	0.000000	*	0.3000	*	serial
2	1	1	0	1	1	1	1	2	0	0.911413		0.9000	*	serial

For further guidelines construct a probability table using the MAPLE program provided in the addendum section of the documentation.

Appendix B

VHDL source code for TRNG

```
-- Title : Test Bench for top_trng
-- Design : sim_trng
-- Author : Jennifer Brady
______
-- File : $DSN\src\TestBench\top_trng_TB.vhd

-- Generated : 10/13/2006, 2:47 AM
-- From : $DSN\src\top.vhd
            : Active-HDL Built-in Test Bench Generator ver. 1.2s
-- Description : Automatically generated Test Bench for top_trng_tb
used to
               simulated a TRNG for a Spartan3 FPGA
______
_____
library ieee, unisim;
use ieee.numeric_std.all;
--use ieee.std_logic_unsigned.all;
--use ieee.std_logic_arith.all;
use ieee.std_logic_1164.all;
use unisim.vcomponents.all;
use math_real.all;
-- Add your library and packages declaration here ...
use std.textio.all;
library
         work;
use work.rng_lib.all;
entity top_trng_tb is
     generic (
     seed1a:positive:=123450;
                                              --initialize seed
values btw 1 and 2147483562
     seed2a:positive:=12340;
     seed3a:positive:=1230;
     seed1b:positive:=120;
     seed2b:positive:=10;
     seed3b:positive:=1);
     endtime:integer:=9999);
end top_trng_tb;
architecture TB_ARCHITECTURE of top_trng_tb is
```

```
-- Component declaration of the tested unit
      component top_trng
      port(
            clk_in : in std_logic;
            clk1 : in std_logic;
            clk0 : in std logic;
            glb_rst : in std_logic;
            strt : in std_logic;
            en_wrout : out std_logic;
            rand_data_out : out std_logic );
      end component;
      -- Stimulus signals - signals mapped to the input and inout ports
of tested entity
      signal clk_in : std_logic;
      signal clk1 : std_logic:='0';
      signal clk0 : std_logic:='0';
      signal glb_rst : std_logic;
      signal strt : std_logic;
      -- Observed signals - signals mapped to the output ports of
tested entity
      signal en_wrout : std_logic;
      signal rand_data_out : std_logic;
      -- Add your code here ...
      signal r_out:std_logic_vector(3 downto 0):=(others=>'0');
      signal genrnd:std_logic_vector(4095 downto 0);
      signal randbits:std_logic_vector(4095 downto 0);
      signal cnt:integer:=0;
      -- additional signals to test design
      signal end_sim:boolean:=false;
      file per0_gt:text open write_mode is "140_12per0rf.txt";
      file per1 gt:text open write mode is "140 12per1rf.txt";
      file rand_out : text open write_mode is
"10nsc_140psf_24jrfout_qa.txt";
begin
      -- Unit Under Test port map
      UUT : top_trng
            port map (
                  clk_in => clk_in,
                  clk1 \Rightarrow clk1,
                  clk0 => clk0,
                  glb_rst => glb_rst,
                  strt => strt,
                  en_wrout => en_wrout,
                  rand_data_out => rand_data_out);
      -- Add your stimulus here ...
      strt<='1';
      r_out(0) <= rand_data_out;
```

```
rst:process
      begin
                              -- reset all components at start up
            glb_rst<='1';
            wait for 20 ns;
            qlb rst<='0';</pre>
            wait;
      end process;
      sys_clk: process
                                --system clk is 50M Hz
      begin
            if end_sim then
                  wait;
            end if;
                  clk_in<='1';
                  wait for 10 ns;
                  clk_in<='0';
                  wait for 10 ns;
      end process sys_clk;
-- a Gaussian pseudo random number generator is used to simulate jitter
on clk --- oscillator edges.
      clk_osc0: process
      variable delta:integer;
      variable seed_la:positive:=seedla;
--initialize seed values btw 1 and 2147483562
      variable seed_2a:positive:=seed2a; -- in generic part of entity
      variable seed 3a:natural:=seed3a;
      variable randg:rand_var;
      variable var_randq_i:real;
      variable rline0: LINE;
      variable rtline0: LINE;
      variable data0:integer;
      constant mu:real:=0.12;
-- mu=.12 for 24 ps, mu=0.35 for 70 ps, mu=0.7 for 140 ps, mu=1 for 200
      constant sigma:real:=1.0;
      begin
                  randg:=
init_gaussian(seed_1a, seed_2a, seed_3a, mu, sigma);
            while not end_sim loop
                  randg:=rand(randg);
                  var_randg_i:=randg.rnd;
                  delta:=integer(round(var randg i*100.0));
--put random number in integer form for indexing loop
                  if 0 <= delta and delta <= 24 then
               --range is width of jitter zone
                        clk0<=not clk0;</pre>
                        wait for 3.692 ns;
                     --min time for half cycle of oscillator
                        data0:=3692+delta;
                        write (rtline0, data0);
                        writeline( per0 qt,rtline0); --output rand# to
file
                  else
                        delta:=0;
                    --if random integer is outside range set loop to 0
```

```
end if;
                          -- and call for a new random value
                  for i in 1 to delta loop
                        wait for 1 ps;
                    -- 1 ps is the most detailed timing allowed. If a
smaller value
                  end loop;
                    --is enter it will round to 1 ps
            end loop;
      end process;
      clk_osc1: process
      variable delta:integer;
      variable seed_lb:positive:=seed1b; --initialize btw 1 and
2147483562
      variable seed_2b:positive:=seed2b;
      variable seed_3b:natural:=seed3b;
     variable randg:rand_var;
     variable var_randg_i:real;
     variable rline1: LINE;
     variable data1:integer;
      variable rtline1: LINE;
      variable trun_rand:integer;
      constant mu:real:=0.12;
      constant sigma:real:=1.0;
      begin
                  randq:=
init_gaussian(seed_1b, seed_2b, seed_3b, mu, sigma);
            while not end_sim loop
                  randg:=rand(randg);
                  var_randg_i:=randg.rnd;
                        write (rline, var_randg_i);
                        writeline( rand_g,rline);
                  delta:=integer(round(var_randg_i*100.0));
--put random number in integer form for indexing loop
                  if 0 <= delta and delta <= 24 then
               --range 2x width of jitter zone
                        clk1<=not clk1;</pre>
                        wait for 3.762 ns;
                     --min time for half cycle of oscillator
                        trun_rand:=delta;
                        data1:=3752+delta;
                        write (rtline1, data1);
                        writeline( perl_gt,rtline1);
                  else
                        delta:=0;
                    --if random integer is outside range set loop to 0
                  end if;
                          -- and call for a new random value
                  for i in 1 to delta loop
                        wait for 1 ps;
                    -- 1 ps is the most detailed timing allowed. If a
smaller value
```

```
end loop;
                    --is enter it will round to 1 ps
            end loop;
      end process;
      write:process(en_wrout,clk_in)
      variable r line: LINE;
      variable int_rand:integer;
      variable wrcnt:integer:=0;
      begin
            if clk_in'event and clk_in='0' then
                  if en_wrout='1' then
                        int_rand:=to_integer(signed(r_out));
                        write (r_line,int_rand);
                        writeline( rand_out,r_line);
                        wrcnt:=wrcnt+1;
                  end if;
            end if;
            cnt<=wrcnt;</pre>
      end process;
      endsimulation:process (clk_in)
      begin
            if clk_in'event and clk_in='1' then
                  cnt<=cnt+1;
                  if cnt=endtime then
                        writeline( rand_out,r_line);
___
                  end if;
            end if;
      end process;
end TB_ARCHITECTURE;
--configuration TESTBENCH_FOR_top_trng of top_trng_tb is
    for TB_ARCHITECTURE
            for UUT : top_trng
                  use entity work.top_trng(top_trng);
            end for;
      end for;
--end TESTBENCH_FOR_top_trng;
```

```
-- Title : top

-- Design : sim_trng

-- Company : USAF
-- File
            : top.vhd
-- Generated : Thu Oct 12 22:07:51 2006
-- From : interface description file
-- By
         : Itf2Vhdl ver. 1.20
______
-- Description : Top level of a true random number generator
              AFIT/Thesis
-- Company:
-- Engineer:
              Jennifer Brady
-- Create Date: 10/12/06
-- Design Name: TRNG
-- Target Device: Spartan3
______
_____
library IEEE;
library work;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.numeric_std.all;
--- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
library UNISIM;
use UNISIM. VComponents.all;
entity top_TRNG is
     port(
     clk_in:in std_logic;
     clk1:in std_logic;
     clk0:in std_logic;
     glb_rst:in std_logic;
     strt:in std_logic;
     en_wrout:out std_logic;
     rand_data_out : out STD_LOGIC);
end top_TRNG;
architecture top_TRNG of top_TRNG is
attribute syn_black_box:boolean;
     -- Component declaration of the "sample(sample)" unit defined in
     component sample
     port(
```

```
reset : in std_logic;
            clk0 : in std_logic;
            clk1 : in std_logic;
            R0 : in std_logic;
            E0 : in std_logic;
            rd ack : in std logic;
            bit_rdy : out std_logic;
            rand_out : out std_logic);
            smpl_out : out std_logic);
      end component;
      -- Component declaration of the "control(control)" unit defined
in
      component control
      port(
            reset : in std_logic;
            clk : in std_logic;
            bit_rdy : in std_logic;
            en_wr : out std_logic;
            rd_ack : out std_logic;
            R0 : out std_logic;
            E0 : out std_logic);
      end component;
      -- Component declaration of the "fdre(fdre_v)" unit defined in
      component fdre
      port(
            Q : out std_ulogic;
            D : in std_ulogic;
            C : in std_ulogic;
            CE : in std_ulogic;
            R : in std_ulogic);
      end component;
signal E0:std_logic;
signal R0:std logic;
signal bit_rdy:std_logic;
signal rand_out:std_logic;
--signal start:std_logic;
signal en_wr:std_logic;
--signal en_rd:std_logic;
signal in_cnt:std_logic_vector(13 downto 0);
signal cnt:std_logic_vector(1 downto 0);
signal rand_data:std_logic_vector(0 downto 0):="0";
--signal wr_ram:std_logic;
signal clk:std_logic;
signal rd_ack:std_logic;
begin
      clk<=clk in;
      en wrout <= en wr;
sam : sample
      port map(
            reset => glb_rst,
```

```
clk0 \Rightarrow clk0,
              clk1 => clk1,
              R0 \Rightarrow R0,
              E0 \Rightarrow E0,
              rd_ack => rd_ack,
              bit_rdy => bit_rdy,
              rand_out => rand_out);
data_cntr : control
      port map(
              reset => glb_rst,
              clk => clk,
              bit_rdy => bit_rdy,
              en_wr=>en_wr,
              rd_ack => rd_ack,
              R0 \Rightarrow R0,
              E0 \Rightarrow E0;
Df_rnd : fdre
       port map(
              Q => rand_data(0),
              D => rand_out,
              C \Rightarrow clk
              CE \Rightarrow R0,
              R => glb_rst);
rand_data_out<=rand_out;</pre>
end top_TRNG;
```

```
-- Company: AFIT/Thesis
-- Engineer: Jennifer Brady
-- Engineer:
-- Create Date: 07/05/05
-- Design Name: TRNG- True Random Number Generator
-- Module Name: sample - sample
-- Project Name:
-- Target Device: Spartan 3
-- Tool versions:
-- Description: uses one clk oscillator to sample a second clk
oscillator on --- the rising edge of the first clk
oscillator
-- Additional Comments:
______
library IEEE;
use IEEE.STD LOGIC 1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
--- Uncomment the following library declaration if instantiating
--- any Xilinx primitives in this code.
library UNISIM;
use UNISIM. VComponents.all;
entity sample is
   Port (
                reset : in std_logic;
                clk0 : in std_logic;
           clk1 : in std_logic;
                 R0:in std_logic;
                 E0:in std_logic;
                 rd ack:in std logic;
                 bit_rdy:out std_logic;
                 rand_out:out std_logic);
                 smpl_out : out std_logic);
end sample;
architecture sample of sample is
     attribute syn_black_box : boolean;
     -- Component declaration of the "fd(fd_v)" unit defined in
     component fd
     port(
           Q : out std_ulogic;
           D : in std_ulogic;
           C : in std_ulogic);
     end component;
     attribute syn_black_box of fd : component is true;
```

```
-- Component declaration of the "fdc_1(fdc_1_v)" unit defined in
      component fdc_1
      port(
             Q : out std_ulogic;
             D : in std ulogic;
             C : in std ulogic;
             CLR : in std_ulogic);
      end component;
      attribute syn_black_box of fdc_1 : component is true;
      -- Component declaration of the "fde(fde_v)" unit defined in
      component fde
      port(
             Q : out std_ulogic;
             D : in std_ulogic;
             C : in std_ulogic;
             CE : in std_ulogic);
      end component;
      attribute syn_black_box of fde : component is true;
  attribute KEEP : string;
signal s0:std_logic;
                                     --clk0 sample
signal CDO:std_logic;
                                     --clk1 divider output
signal N CDO:std logic;
                                      --inverted CDO
signal N_E0:std_logic;
signal clr_bit:std_logic;
--signal rndbit_rdy:std_logic;
--attribute KEEP of rndbit_rdy:signal is "TRUE";
attribute KEEP of bit_rdy:signal is "TRUE";
begin
--smpl_out<=s0;
N_CDO<= not CDO;
N_E0 \le not E0;
clr_bit<=rd_ack or reset;</pre>
--bit_rdy<=rndbit_rdy;</pre>
      clksamp : fd
      port map(
             Q \Rightarrow s0,
             D \Rightarrow clk0,
             C \Rightarrow clk1);
      clk_div : fdc_1
      port map(
             Q => CDO,
             D => N CDO,
             C \Rightarrow clk1,
             CLR \Rightarrow R0);
      bt_rdy: process(s0,N_E0,clr_bit)
```

```
begin
      if clr_bit='1' then
             rndbit_rdy<='0';</pre>
      elsif s0'event and s0='1' then
             if N_E0='1' then
--
                  rndbit_rdy<='1';
             end if;
___
      end if;
      end process bt_rdy;
      FDBR : fdce
      port map(
             Q => bit_rdy,
             D => '1',
             C \Rightarrow s0,
             CE \Rightarrow N_E0,
             CLR =>clr_bit);
      FRO : fde
      port map(
             Q => rand_out,
             D => CDO,
             C \Rightarrow s0,
             CE \Rightarrow N_E0);
end sample;
```

```
______
-- Title
           : control
           : TRNG
-- Design
-- Design : IRNG

-- Author : Jennifer Brady

-- Company : AFIT Thesis
______
_____
-- File : control.vhd
-- Generated :
-- From : interface description file
-- Ву
           : Itf2Vhdl ver. 1.20
______
-- Description : Control circuit code adapted from code created by Paul
Kohlbrenner's
                    top level new_xpv_circuit.vhd for his thesis
titled Design and Analysis of a True
                    Random Number Generator in a Field
Programmable Gate Array
______
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD LOGIC ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
--- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
library UNISIM;
use UNISIM. VComponents.all;
entity control is
     port(
          reset: in STD LOGIC;
          clk : in STD_LOGIC;
          bit_rdy : in STD_LOGIC;
          rand_out : in STD_LOGIC;
          smpl_out : in STD_LOGIC;
          gate_file: in STD_LOGIC;
          gate_con: out STD_LOGIC;
          en_wr : out STD_LOGIC;
          rd_ack : out STD_LOGIC;
          R0 : out STD_LOGIC;
          E0 : out STD_LOGIC);
end control;
```

```
architecture control of control is
signal rst_bit_rdy:std_logic;
signal en_rnd:std_logic;
signal ds enrnd:std logic;
signal rnd_ack:std_logic;
begin
      process(reset, bit_rdy, rst_bit_rdy)
            begin
                  if reset='1' then
                         en_rnd<='0';
                  elsif rst_bit_rdy='1' then
                         en_rnd<='0';
                  elsif bit_rdy'event and bit_rdy='1' then
                         en_rnd<='1' ;
                  end if;
            end process;
      process(reset,clk,en_rnd,ds_enrnd)
            begin
                  if reset='1' then
                        rst_bit_rdy<='0';
                         ds enrnd<='0';
                  elsif clk'event and clk='1' then
                         if ds_enrnd='1' then
                               ds_enrnd<='0';
                         elsif en\_rnd='1' then
                               ds_enrnd<='1';
                               rst_bit_rdy<='1';</pre>
                         else
                               rst_bit_rdy<='0';</pre>
                         end if;
                  end if;
      end process;
      process(reset,en_rnd,rst_bit_rdy)
            begin
                  if reset='1' then
                         E0<='0';
                         R0<='0';
                  else
                         E0<=en_rnd or rst_bit_rdy;
                         R0<=en_rnd;
                  end if;
            end process;
            rd_ack<=rst_bit_rdy;
            en wr<=ds enrnd;
end control;
```

```
_____
-- Company:
                AFIT/Thesis
                Jennifer Brady
-- Engineer:
-- Create Date:
                07/05/05
-- Design Name: TRNG- True Random Number Generator
-- Module Name: sample2 - sample
-- Project Name:
-- Target Device: Spartan 3
-- Tool versions:
-- Description: Uses one oscillator to sample the a second oscillator
                                 on the rising and falling edge of
the first oscillator
-- Dependencies:
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
______
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
--- Uncomment the following library declaration if instantiating
--- any Xilinx primitives in this code.
library UNISIM;
use UNISIM. VComponents.all;
entity sample is
   Port (
                reset : in std_logic;
                clk0 : in std_logic;
               clk1 : in std_logic;
                 R0:in std_logic;
                 E0:in std_logic;
                 rd_ack:in std_logic;
                bit_rdy:out std_logic;
                 rand_out:out std_logic
                 smpl_out : out std_logic
                  );
end sample;
architecture sample of sample is
     attribute syn_black_box : boolean;
      -- Component declaration of the "fd(fd_v)" unit defined in
```

```
port(
            Q : out std_ulogic;
            D : in std_ulogic;
            C : in std_ulogic);
      end component;
      attribute syn_black_box of fd : component is true;
      -- Component declaration of the "fdc_1(fdc_1_v)" unit defined in
      component fdc_1
      port(
            Q : out std_ulogic;
            D : in std_ulogic;
            C : in std_ulogic;
            CLR : in std_ulogic);
      end component;
      attribute syn_black_box of fdc_1 : component is true;
      -- Component declaration of the "fde(fde_v)" unit defined in
      component fde
      port(
            Q : out std_ulogic;
            D : in std_ulogic;
            C : in std_ulogic;
            CE : in std_ulogic);
      end component;
      attribute syn_black_box of fde : component is true;
      -- Component declaration of the "fd_1(fd_1_v)" unit defined in
      -- file: "./src/spartan3.vhd"
      component fd_1
      port(
            Q : out std_ulogic;
            D : in std ulogic;
            C : in std_ulogic);
      end component;
      attribute syn black box of fd 1 : component is true;
  attribute KEEP : string;
                                  --clk0 sample
--clk1 divider output
signal s0_r:std_logic;
signal rCDO:std_logic;
signal rN_CDO:std_logic;
                                         --inverted CDO
signal fCDO:std_logic;
                                    --clk1 divider output
signal fN_CDO:std_logic;
                                        --inverted CDO
--signal N_E0_r:std_logic;
--signal clr_bit_r:std_logic;
signal bit_rdy_r:std_logic;
--signal bit_rdy_r:std_logic;
signal s0_f:std_logic;
                                    --clk0 sample
--signal N_E0_f:std_logic;
--signal clr_bit_f:std_logic;
signal bit rdy f:std logic;
signal bit_rdy_w:std_logic;
--signal bit_rdy_f:std_logic;
signal N_E0:std_logic;
```

component fd

```
signal clr_bit:std_logic;
signal rand_r:std_logic;
signal rand_f:std_logic;
signal R0r:std_logic;
signal r_out:std_logic:='0';
attribute KEEP of bit_rdy_r:signal is "TRUE";
attribute KEEP of bit_rdy_f:signal is "TRUE";
begin
--smpl_out<=s0;
rN_CDO<= not rCDO;
fN_CDO<= not fCDO;
N_E0 \le not E0;
clr_bit<=rd_ack or reset;</pre>
bit_rdy<=bit_rdy_r or bit_rdy_f ;</pre>
bit_rdy_w<=bit_rdy_r or bit_rdy_f;
R0r<= R0 or reset;
       clksamp_r : fd
       port map(
              Q \Rightarrow s0_r
              D \Rightarrow clk0,
              C \Rightarrow clk1);
       clk_divr : fdc_1
       port map(
              Q \Rightarrow rCDO,
              D \Rightarrow rN\_CDO,
              C \Rightarrow clk1,
              CLR \Rightarrow ROr);
       bt_rdy_r: process(s0_r,N_E0,clr_bit)
       begin
       if clr bit='1' then
              rndbit_rdy_r<='0';</pre>
       elsif s0_r'event and s0_r='1' then
___
              if N_E0='1' then
                     rndbit_rdy_r<='1';</pre>
              end if;
___
       end if;
       end process bt_rdy_r;
       FDBR_r : fdce
       port map(
              Q => bit_rdy_r,
              D => '1',
              C \Rightarrow s0_r
              CE \Rightarrow N_E0,
              CLR =>clr_bit);
       FRO1 : fde
       port map(
              Q => rand_r,
              D \Rightarrow rCDO,
```

```
C \Rightarrow s0_r
              CE \Rightarrow N_E0;
       -- sampling on the negative edge
       clksamp_f : fd_1
       port map(
              Q \Rightarrow s0_f
              D \Rightarrow clk0,
              C \Rightarrow clk1);
       clk_divf : fdc
       port map(
              Q \Rightarrow fCDO,
              D \Rightarrow fN_CDO,
              C \Rightarrow clk1,
              CLR \Rightarrow ROr);
       bt_rdy_f: process(s0_f,N_E0,clr_bit)
       begin
       if clr_bit='1' then
              rndbit_rdy_f<='0';</pre>
       elsif s0_f'event and s0_f='1' then
              if N_E0='1' then
___
                      rndbit_rdy_f<='1';</pre>
___
              end if;
       end if;
       end process bt_rdy_f;
___
       FDBR_f : fdce
       port map(
              Q => bit_rdy_f,
              D => '1',
              C \Rightarrow s0_f
              CE \Rightarrow N_E0,
              CLR =>clr bit);
       FRO2 : fde
       port map(
              Q \Rightarrow rand_f,
              D \Rightarrow fCDO,
              C \Rightarrow s0_f
              CE \Rightarrow N_E0);
       process
              begin
                      if reset='1' then
                             r_out<='0';
                      else
                             wait until bit_rdy_w'event and bit_rdy_w='1';
                             if bit_rdy_r='1' then
                                    r_out<=rand_r;
                             elsif bit rdy f='1' then
                                     r_out<=rand_f;
                             else
                             end if;
```

```
end if;
end process;

rand_out<=r_out;</pre>
```

end sample;

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